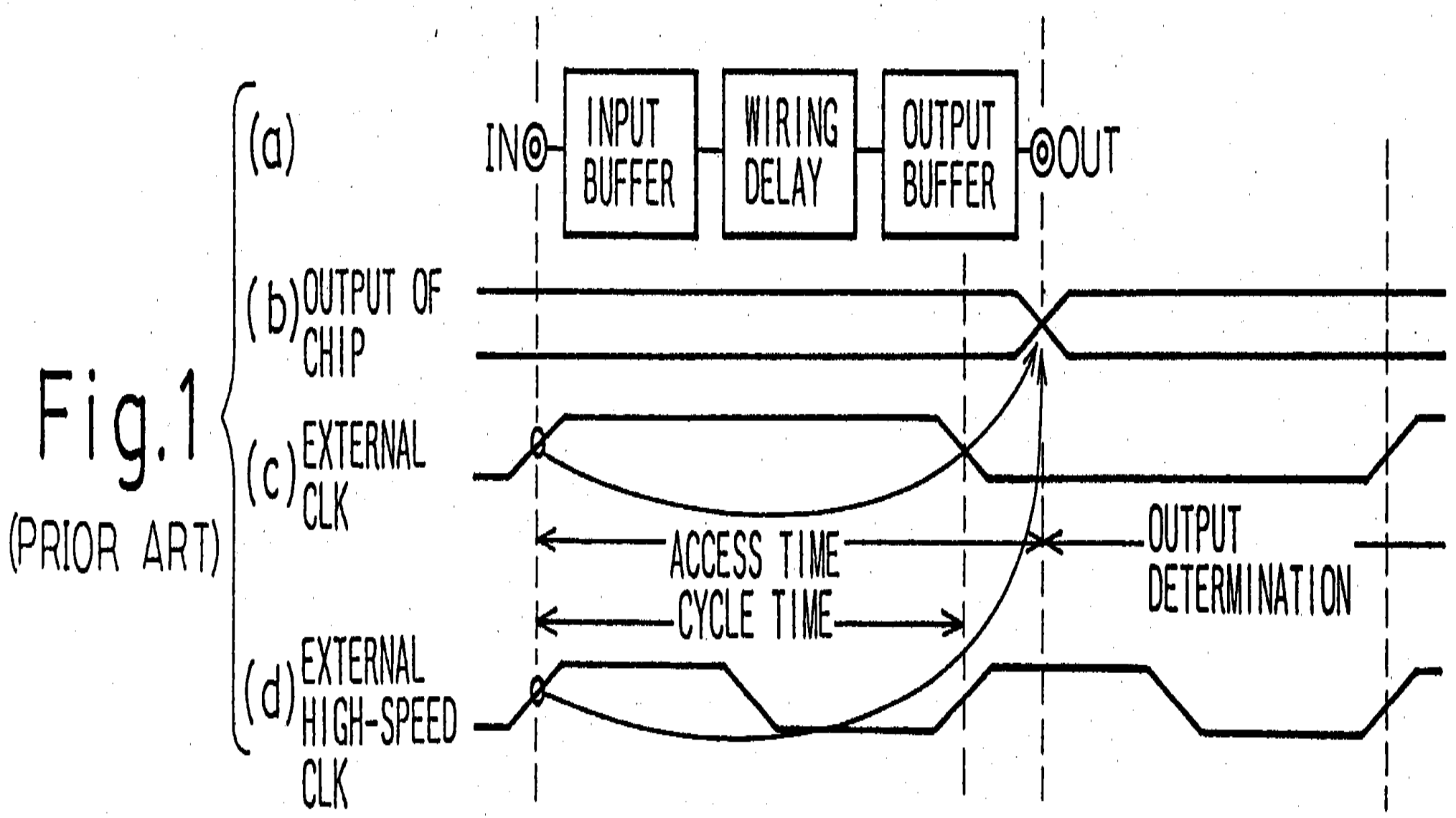


Fig.1
(PRIOR ART)

Fig.2 (PRIOR ART)

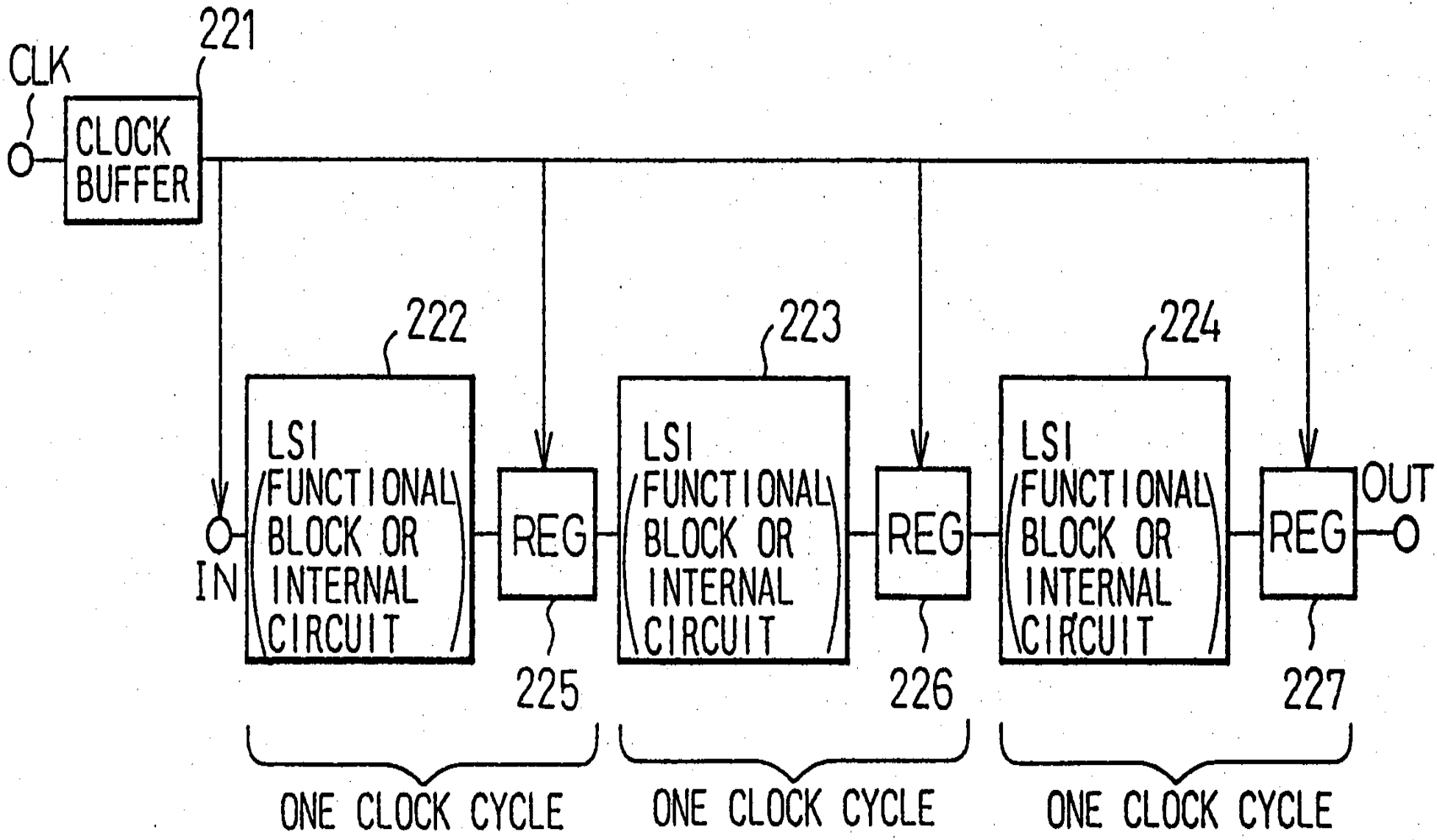


Fig.3(PRIOR ART)

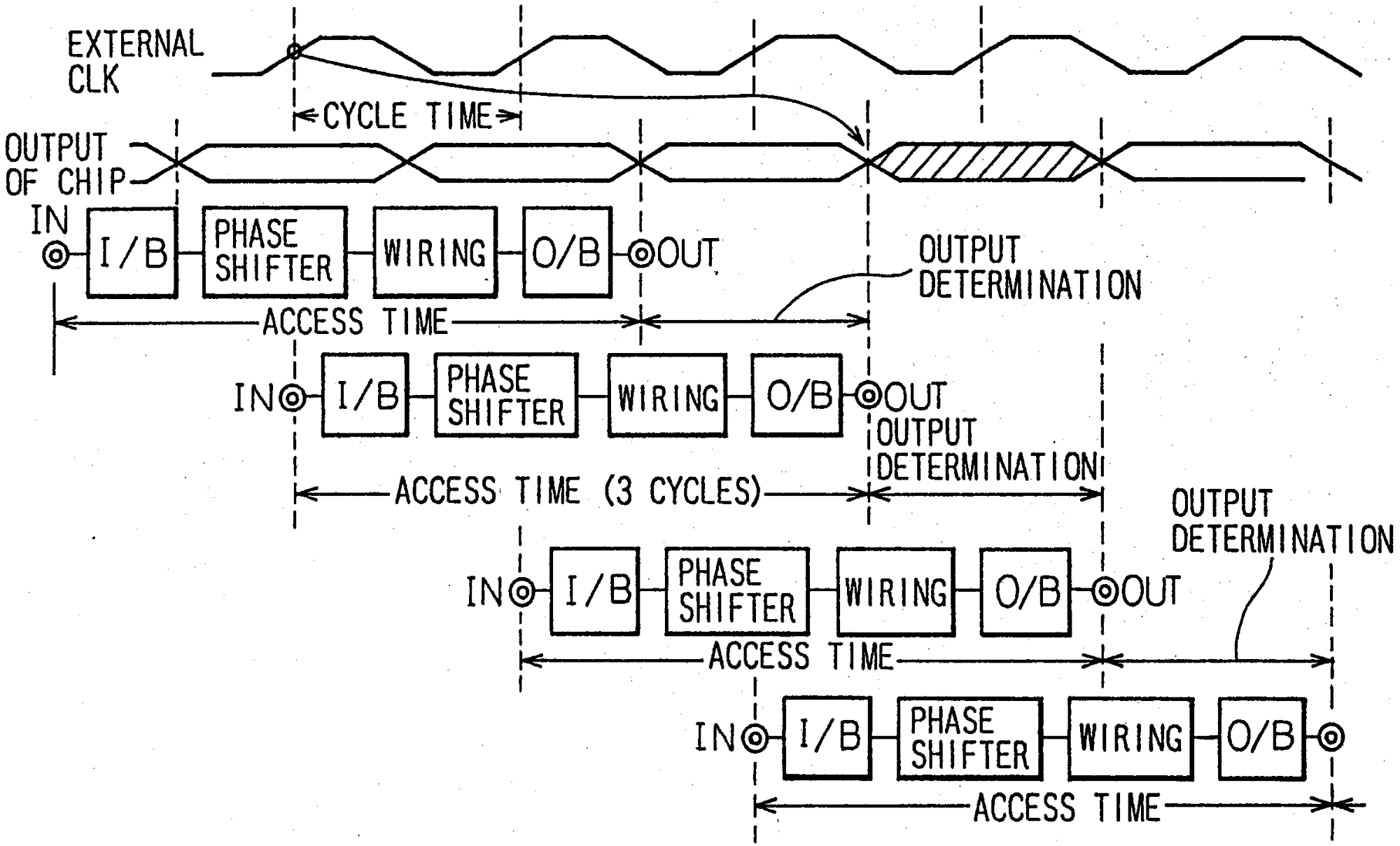


Fig.4

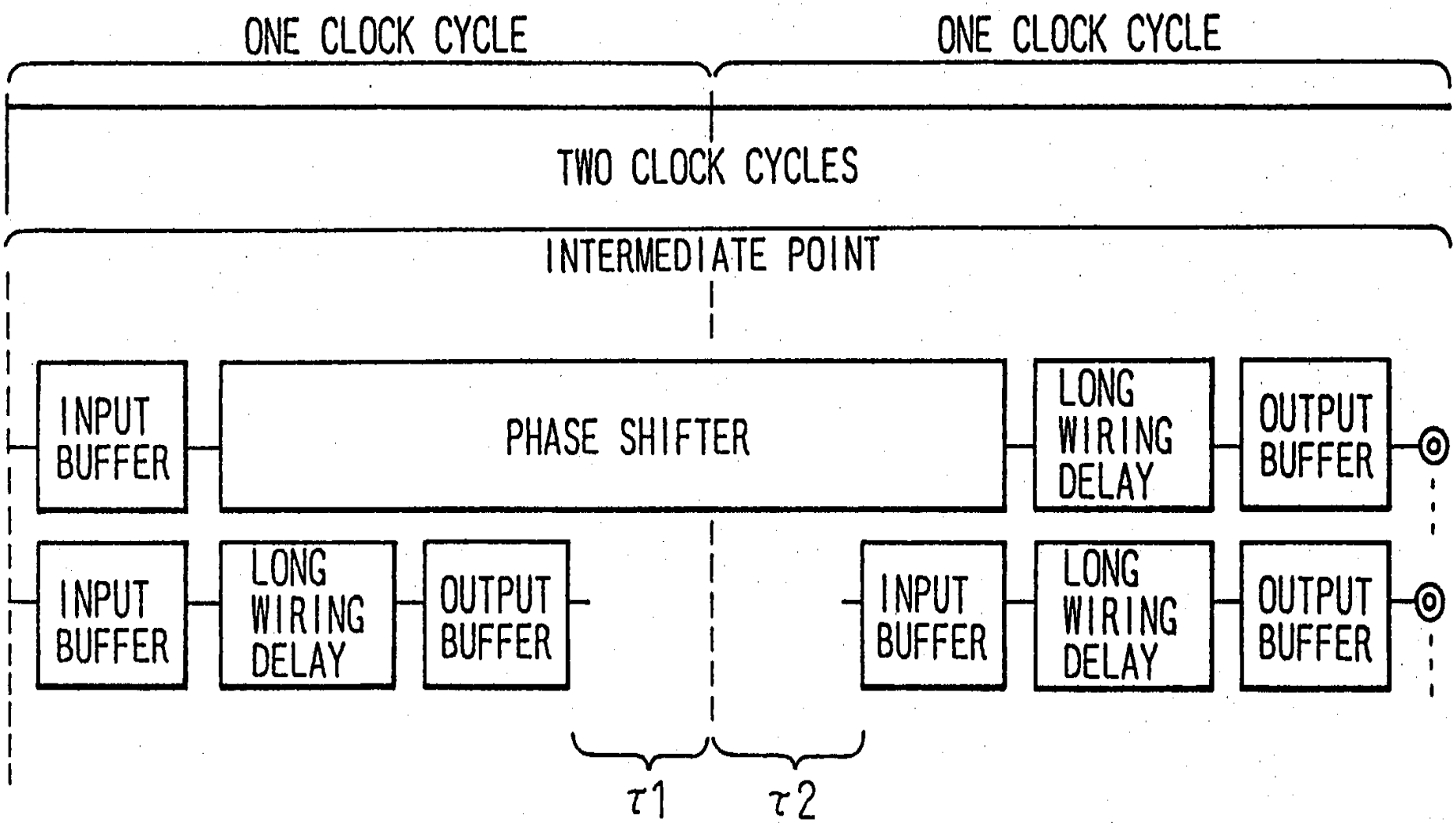

ONE CLOCK CYCLE
ONE CLOCK CYCLE
TWO CLOCK CYCLES
INTERMEDIATE POINT
INPUT BUFFER
PHASE SHIFTER
LONG WIRING DELAY
OUTPUT BUFFER
INPUT BUFFER
LONG WIRING DELAY
OUTPUT BUFFER
INPUT BUFFER
LONG WIRING DELAY
OUTPUT BUFFER
τ1
τ2

Fig.5

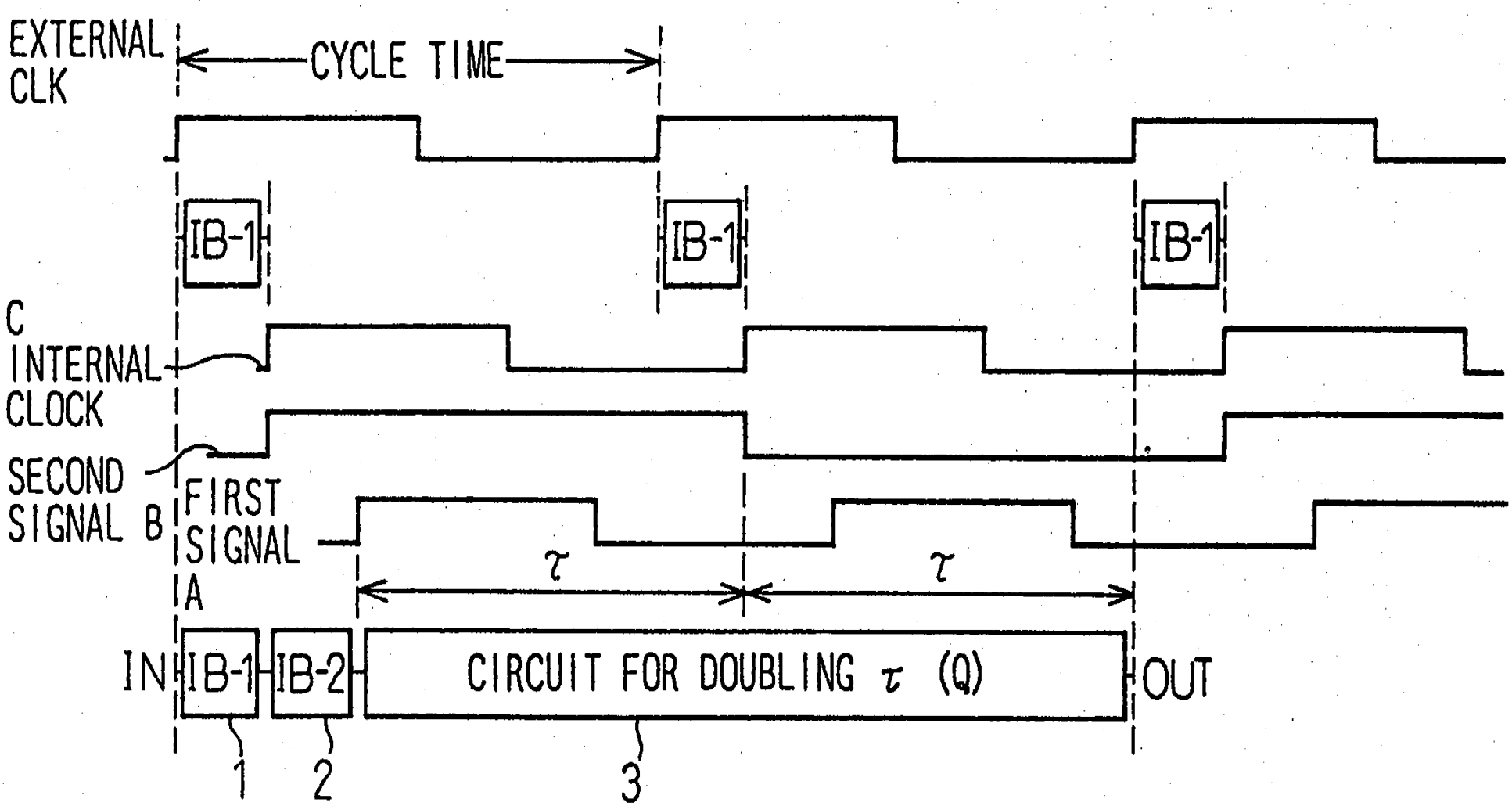

EXTERNAL CLK
CYCLE TIME
IB-1
IB-1
IB-1
C
INTERNAL CLOCK
SECOND SIGNAL B
FIRST SIGNAL A
τ
τ
IN
IB-1
IB-2
CIRCUIT FOR DOUBLING τ (Q)
OUT
1
2
3

Fig.6

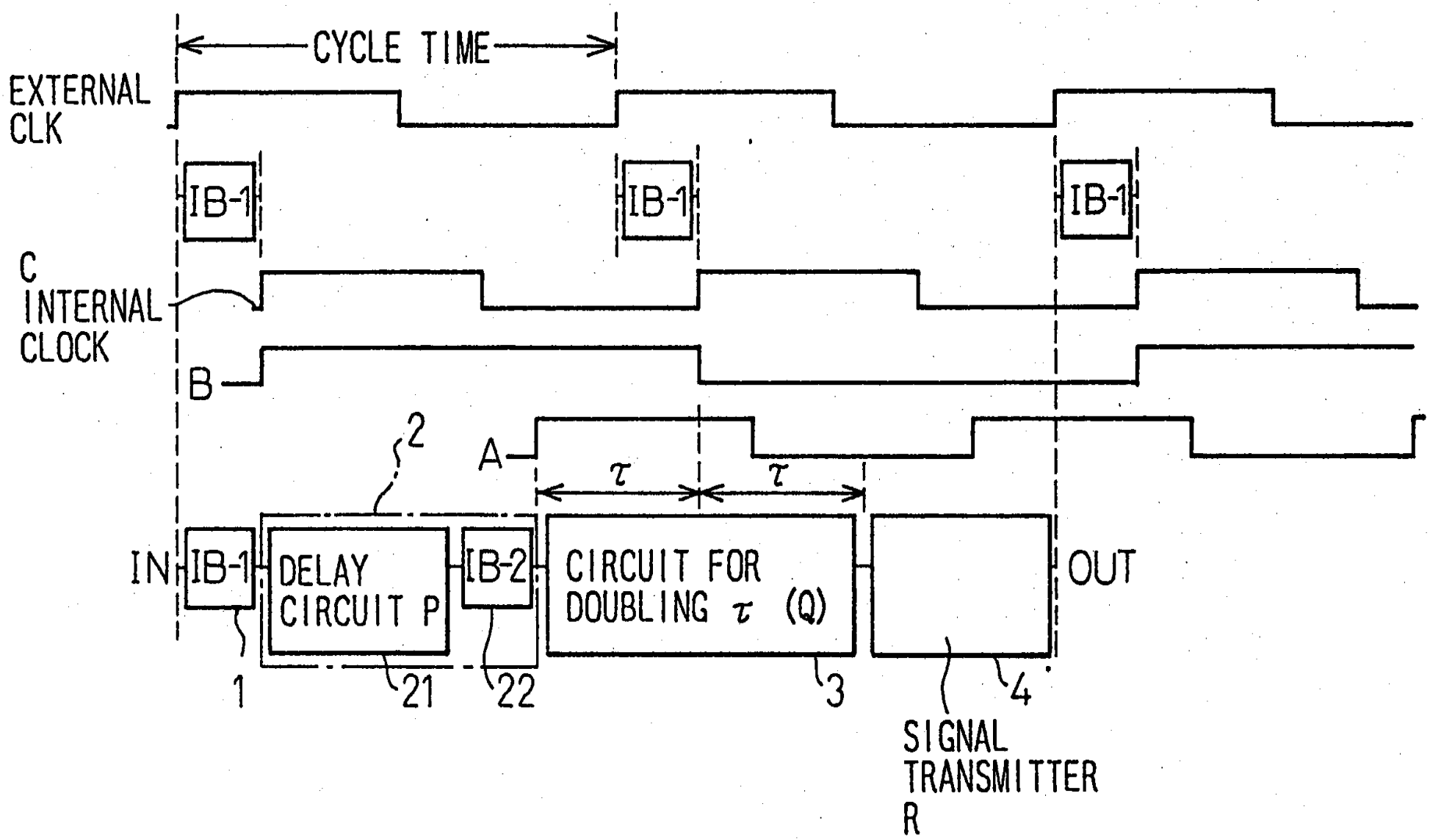

CYCLE TIME
EXTERNAL CLK
IB-1
IB-1
IB-1
C
INTERNAL CLOCK
B
A
2
τ
τ
IN
IB-1
DELAY CIRCUIT P
IB-2
CIRCUIT FOR DOUBLING τ (Q)
OUT
1
21
22
3
4
SIGNAL TRANSMITTER R

Fig.7

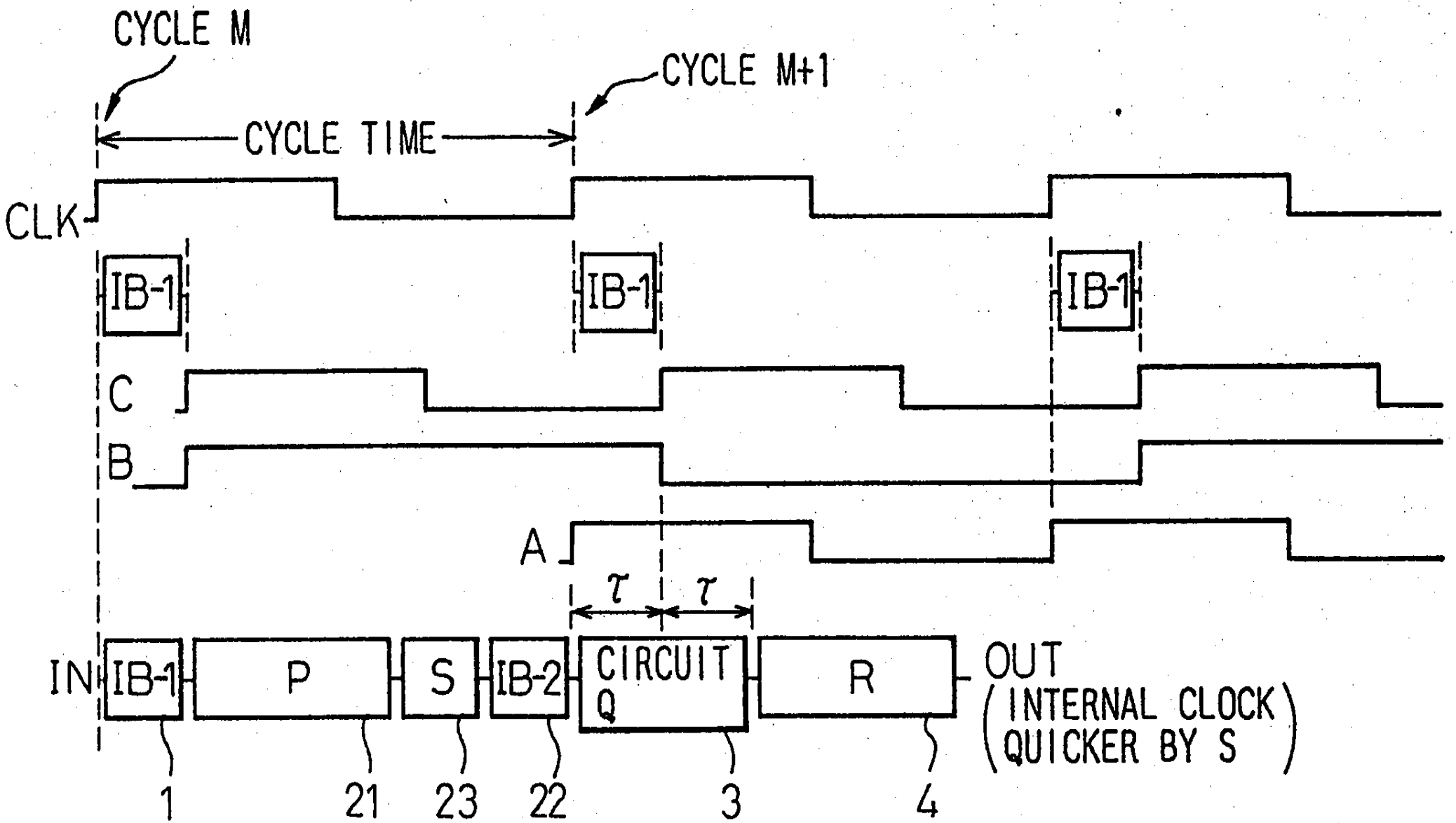

CYCLE M
CYCLE M+1
CYCLE TIME
CLK
IB-1
IB-1
IB-1
C
B
A
τ
τ
IN
IB-1
P
S
IB-2
CIRCUIT Q
R
OUT
(INTERNAL CLOCK QUICKER BY S)
1
21
23
22
3
4

Fig.8

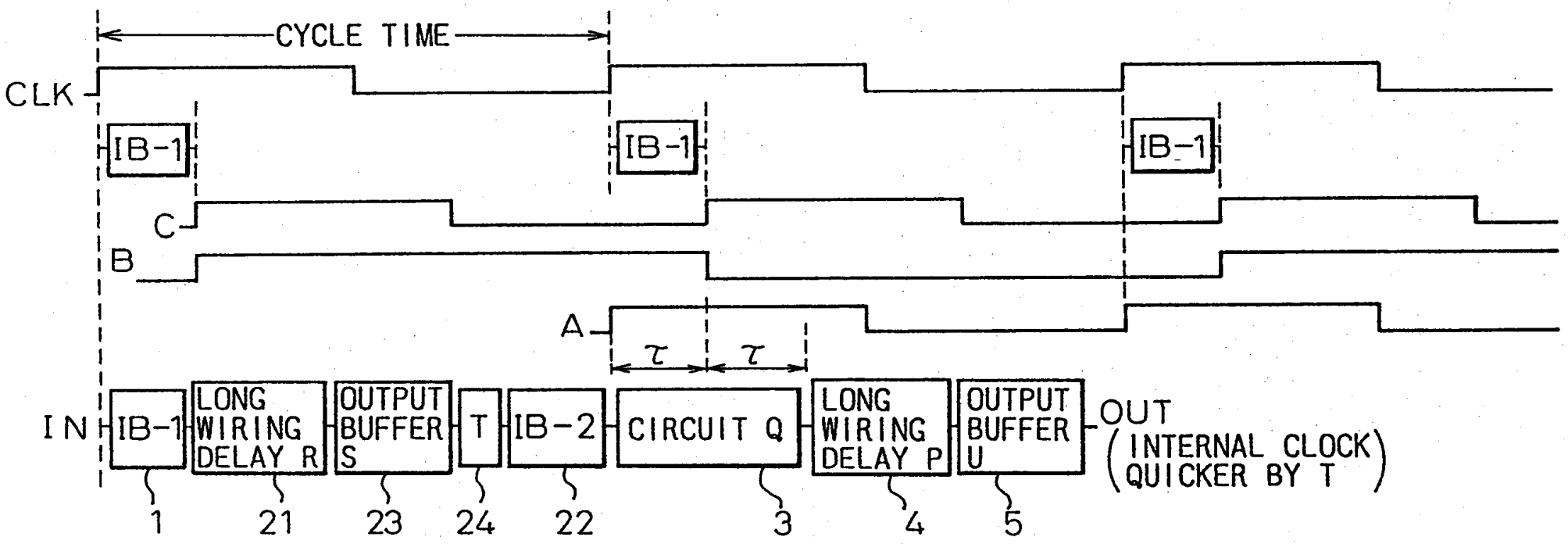

CYCLE TIME
CLK
IB-1
IB-1
IB-1
C
B
A
τ
τ
IN
IB-1
LONG WIRING DELAY R
OUTPUT BUFFER S
T
IB-2
CIRCUIT Q
LONG WIRING DELAY P
OUTPUT BUFFER U
OUT
(INTERNAL CLOCK QUICKER BY T)
1
21
23
24
22
3
4
5

Fig.9

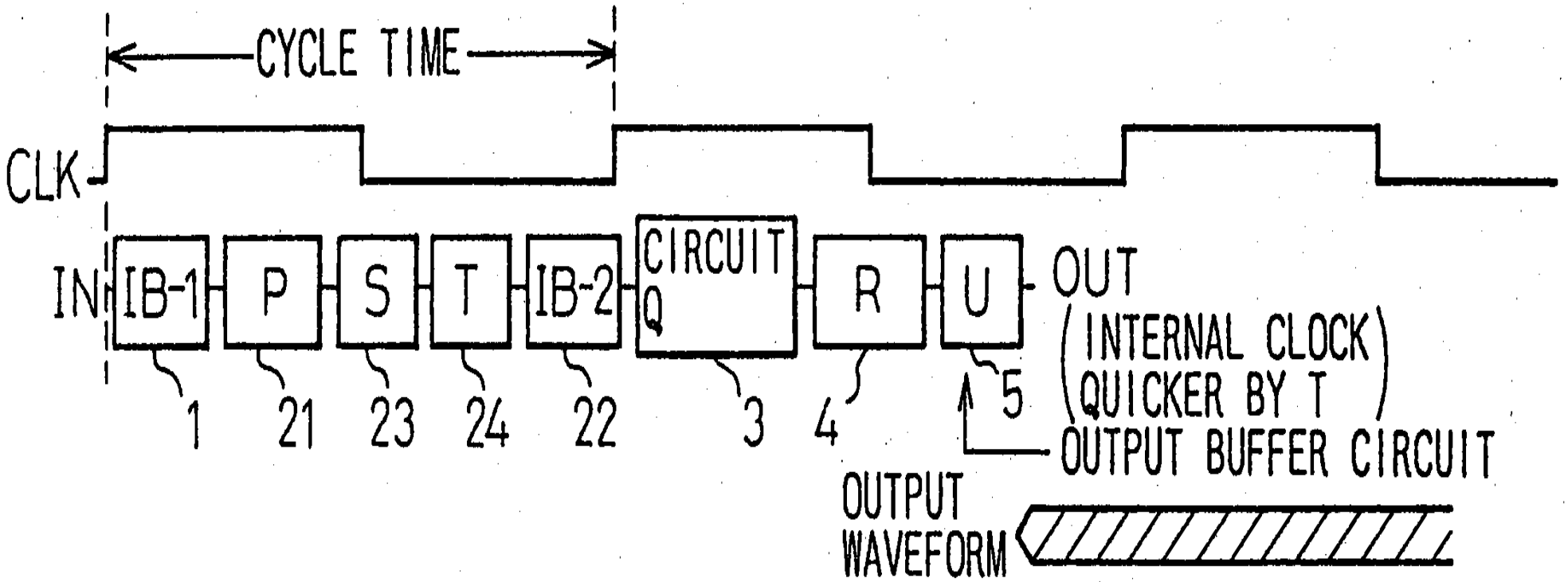

CYCLE TIME
CLK
IN
IB-1
P
S
T
IB-2
CIRCUIT
Q
R
U
OUT
(INTERNAL CLOCK
QUICKER BY T)
OUTPUT BUFFER CIRCUIT
1
21
23
24
22
3
4
5
OUTPUT
WAVEFORM

Fig.10

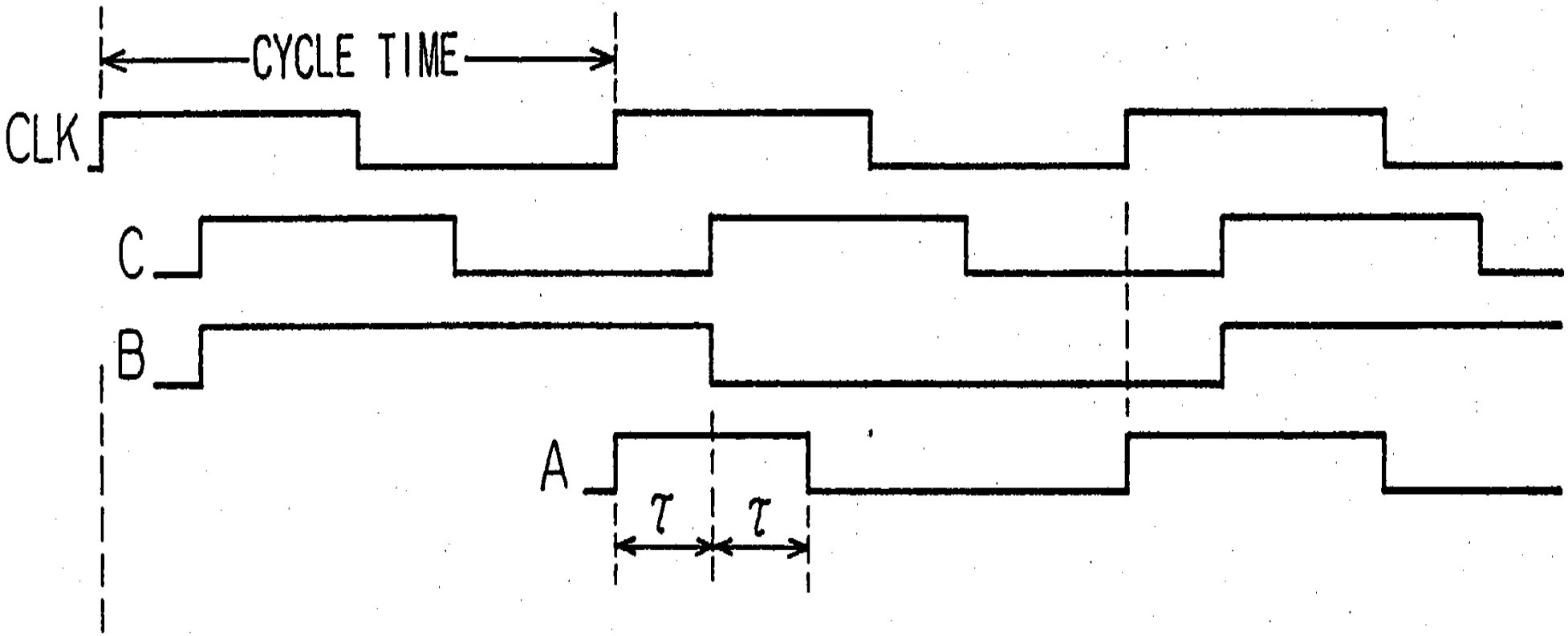


Fig.11

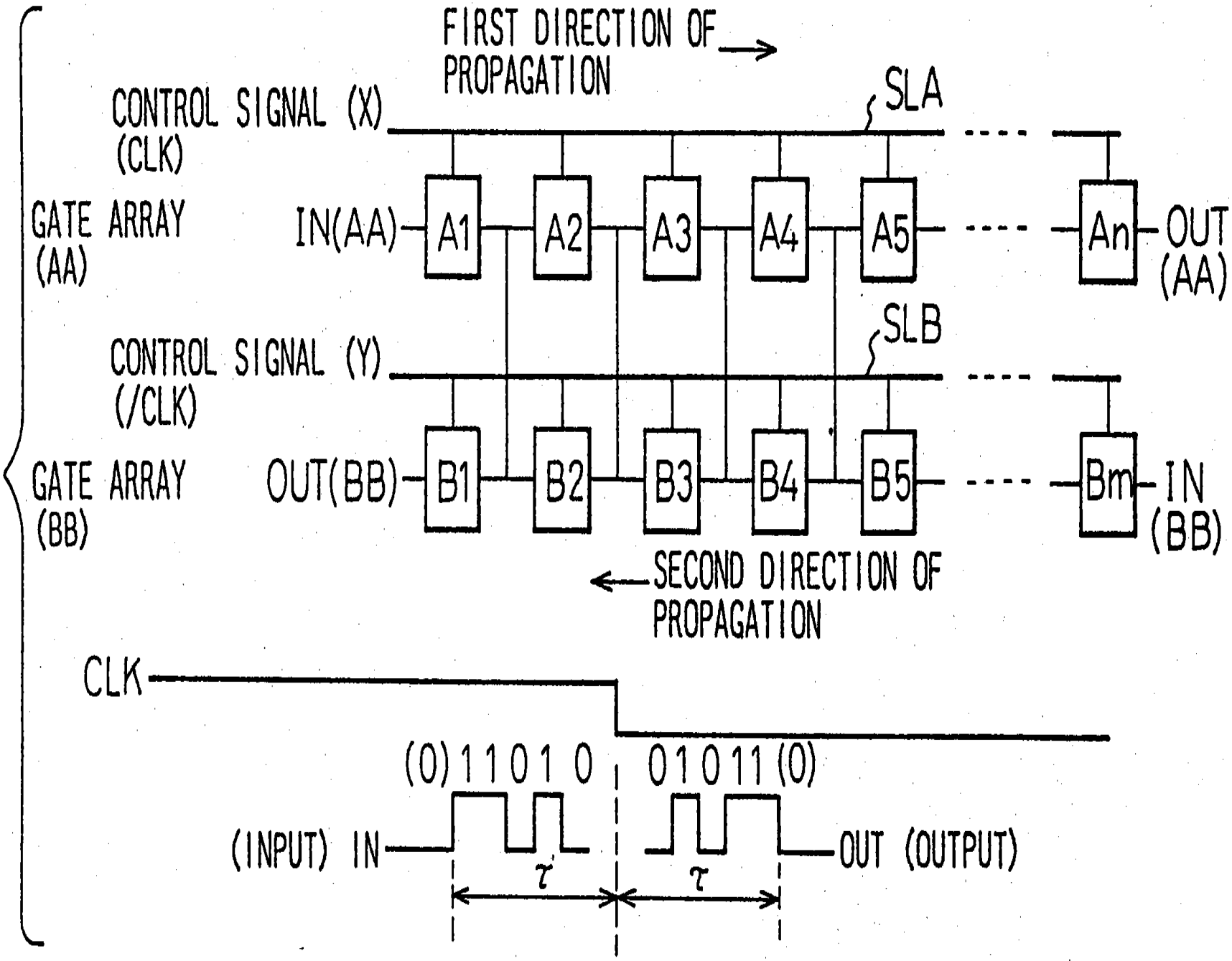

FIRST DIRECTION OF PROPAGATION
CONTROL SIGNAL (X) (CLK)
SLA
GATE ARRAY (AA)
IN(AA)
A1
A2
A3
A4
A5
An
OUT (AA)
CONTROL SIGNAL (Y) (/CLK)
SLB
GATE ARRAY (BB)
OUT(BB)
B1
B2
B3
B4
B5
Bm
IN (BB)
SECOND DIRECTION OF PROPAGATION
CLK
(0)11010
01011(0)
(INPUT) IN
OUT (OUTPUT)
τ
τ

Fig.12

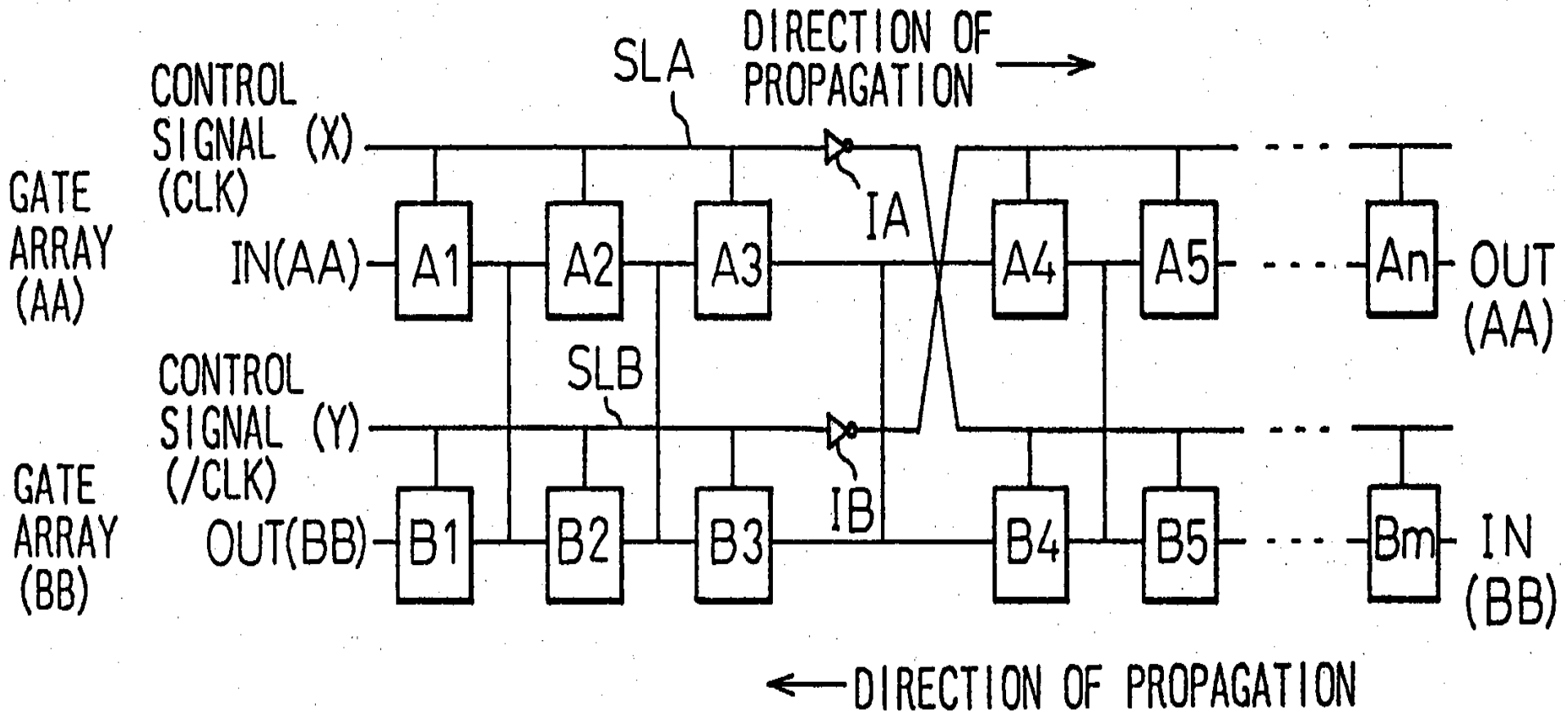

DIRECTION OF PROPAGATION
SLA
CONTROL SIGNAL (X) (CLK)
GATE ARRAY (AA)
IN(AA)
A1
A2
A3
IA
A4
A5
An
OUT (AA)
CONTROL SIGNAL (Y) (/CLK)
SLB
GATE ARRAY (BB)
OUT(BB)
B1
B2
B3
IB
B4
B5
Bm
IN (BB)
DIRECTION OF PROPAGATION

Fig.13

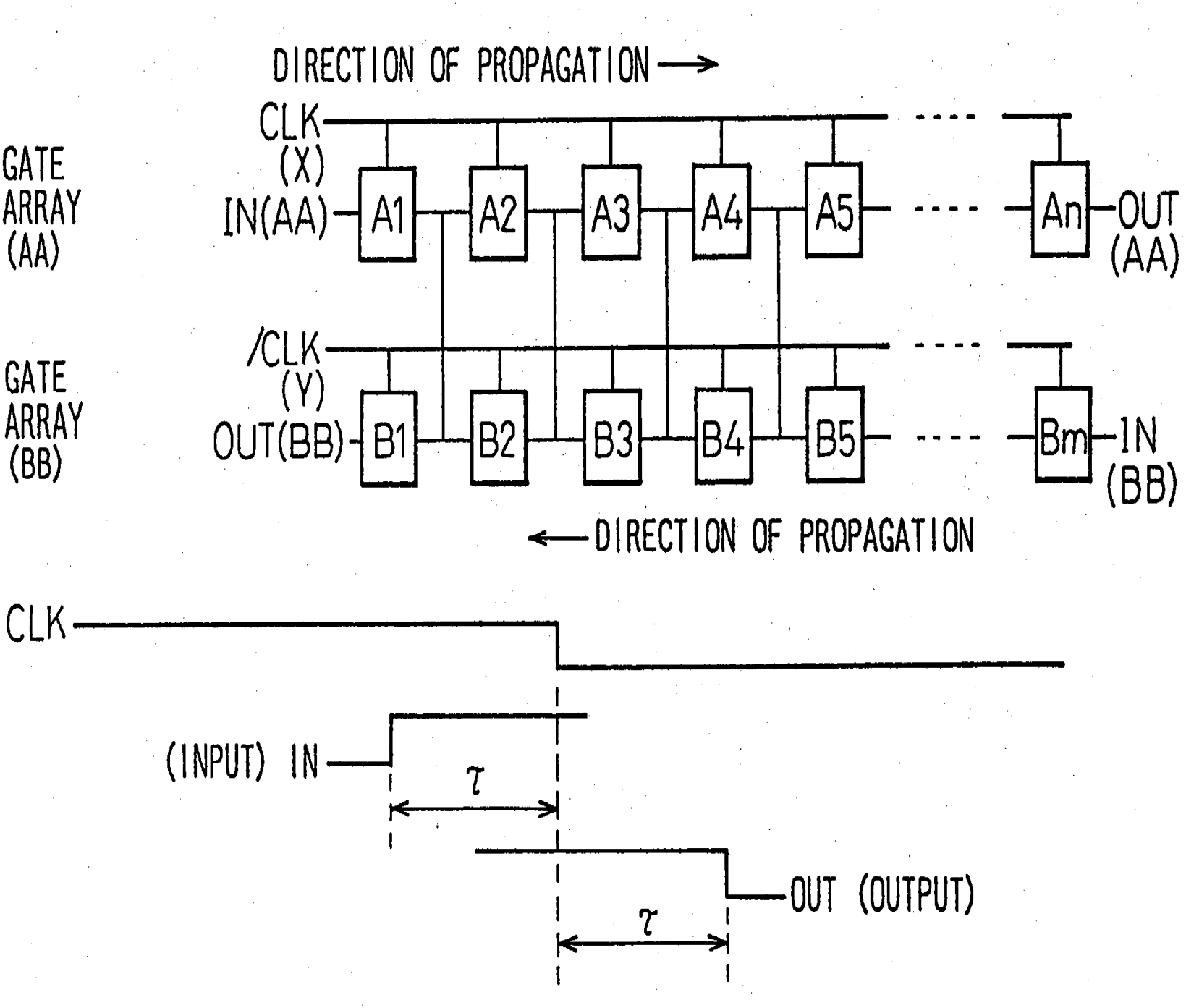
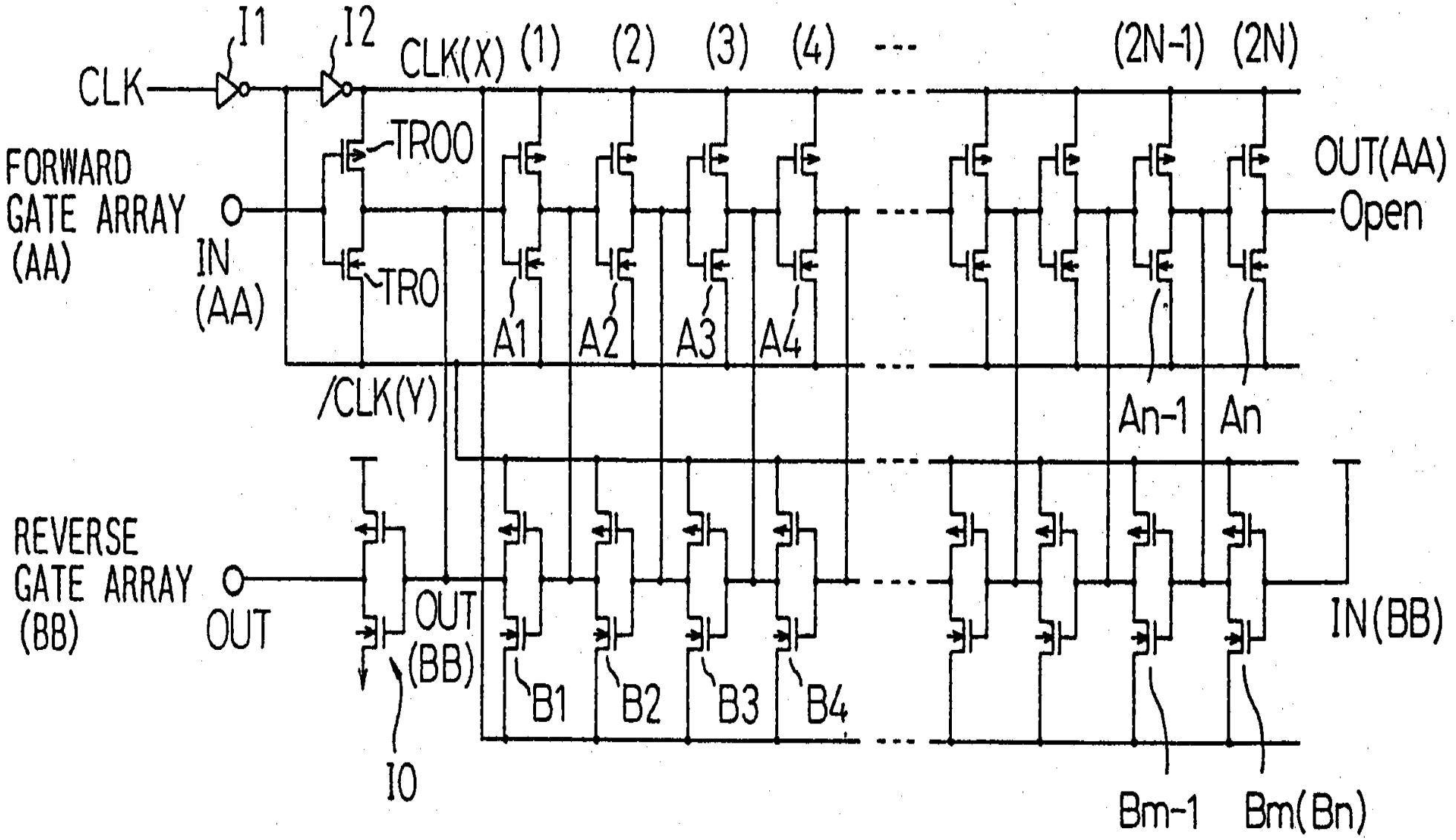
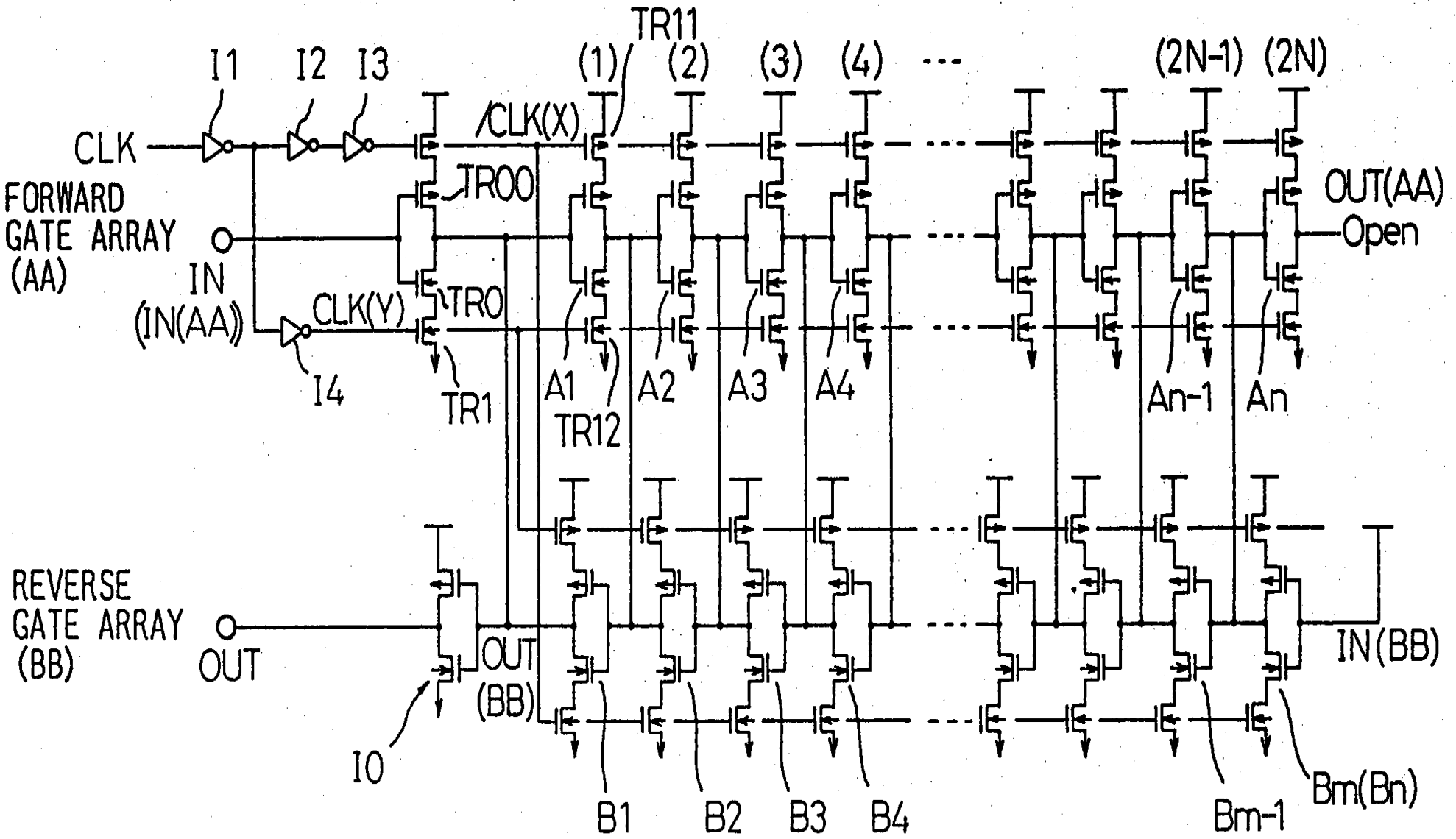

DIRECTION OF PROPAGATION
CLK
(X)
GATE
ARRAY
(AA)
IN(AA)
A1
A2
A3
A4
A5
An
OUT
(AA)
/CLK
(Y)
GATE
ARRAY
(BB)
OUT(BB)
B1
B2
B3
B4
B5
Bm
IN
(BB)
DIRECTION OF PROPAGATION
CLK
(INPUT) IN
τ
OUT (OUTPUT)
τ

Fig.14


I1
I2
CLK
CLK(X)
(1)
(2)
(3)
(4)

(2N-1)
(2N)
TR00
FORWARD
GATE ARRAY
(AA)
IN
(AA)
TR0
OUT(AA)
Open
A1
A2
A3
A4
/CLK(Y)
An-1
An
REVERSE
GATE ARRAY
(BB)
OUT
OUT
(BB)
B1
B2
B3
B4
IN(BB)
I0
Bm-1
Bm(Bn)

Fig.15


I1
I2
I3
TR11
(1)
(2)
(3)
(4)

(2N-1)
(2N)
CLK
/CLK(X)
TR00
FORWARD
GATE ARRAY
(AA)
IN
(IN(AA))
CLK(Y)
TR0
I4
TR1
A1
TR12
A2
A3
A4
An-1
An
OUT(AA)
Open
REVERSE
GATE ARRAY
(BB)
OUT
OUT
(BB)
IN(BB)
I0
B1
B2
B3
B4
Bm-1
Bm(Bn)

Fig.16

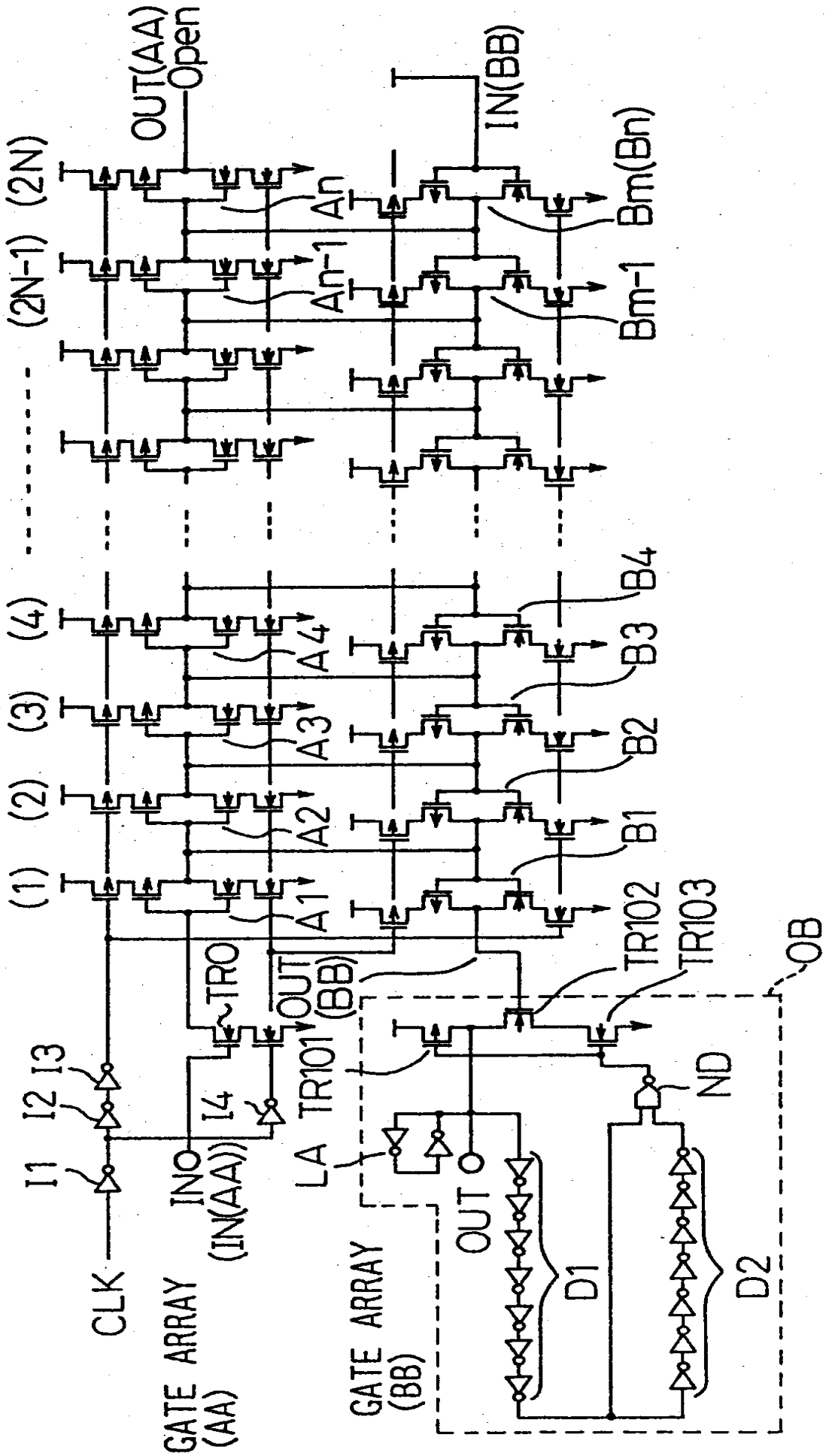

OUT(AA)
Open
IN(BB)
(2N)
(2N-1)
An
An-1
Bm(Bn)
Bm-1
(4)
(3)
(2)
(1)
A4
A3
A2
A1
B4
B3
B2
B1
TR0
OUT
(BB)
TR101
TR102
TR103
OB
I1
I2
I3
I4
IN0
(IN(AA))
LA
ND
CLK
GATE ARRAY
(AA)
GATE ARRAY
(BB)
OUT
D1
D2

Fig.17

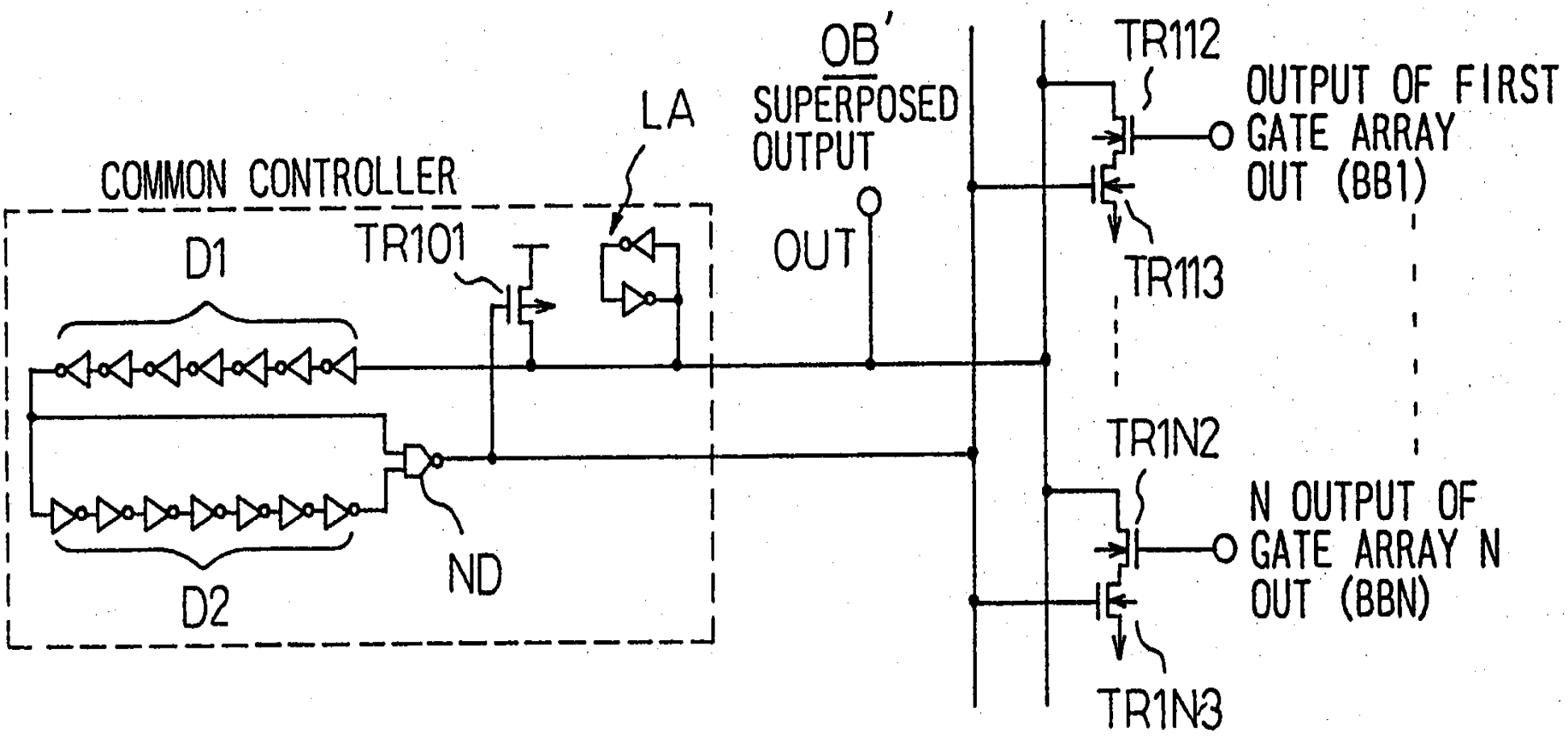

COMMON CONTROLLER
D1
D2
TR101
LA
ND
OUT
OB'
SUPERPOSED OUTPUT
TR112
TR113
TR1N2
TR1N3
OUTPUT OF FIRST GATE ARRAY OUT (BB1)
N OUTPUT OF GATE ARRAY N OUT (BBN)

Fig.18

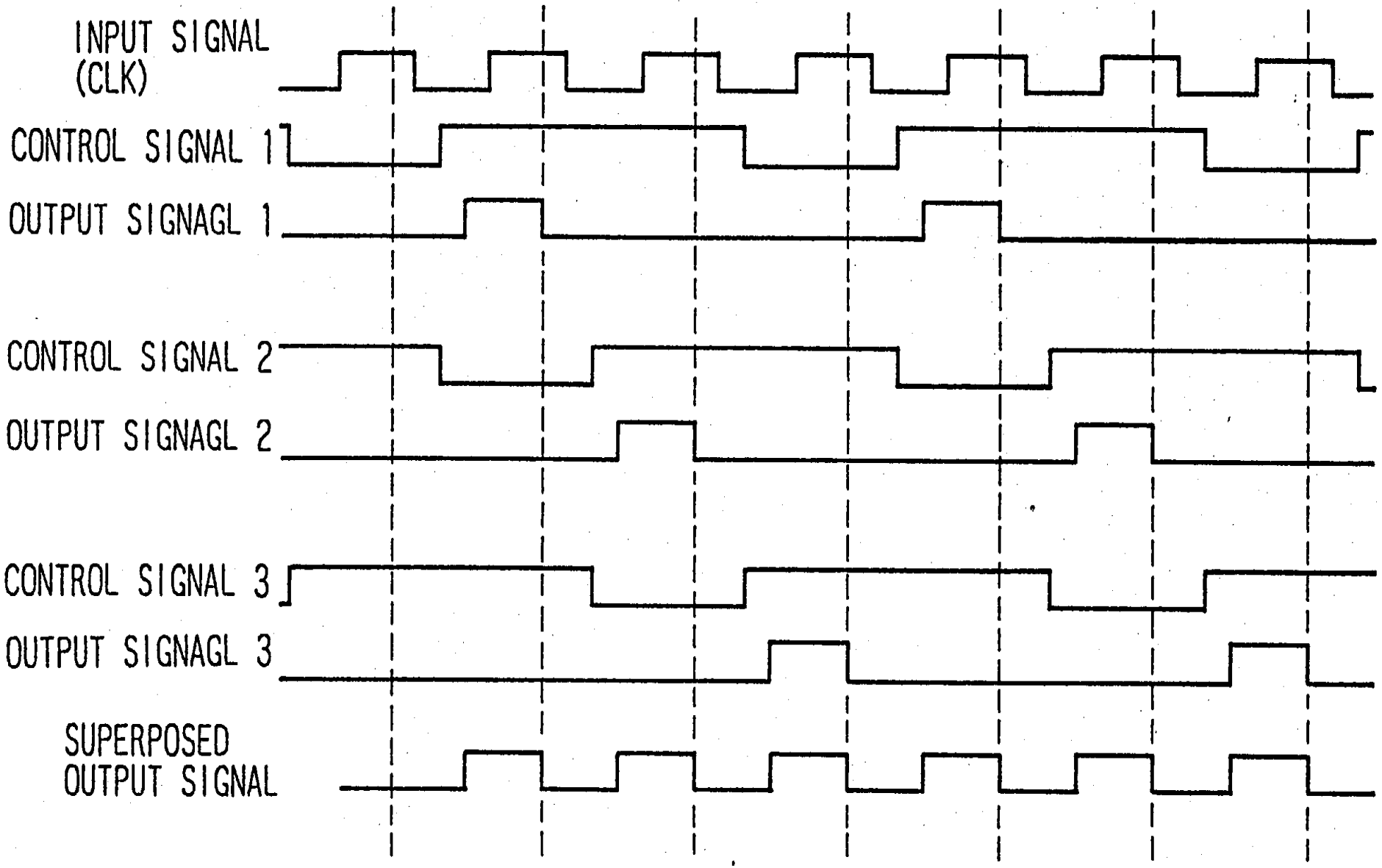

INPUT SIGNAL
(CLK)
CONTROL SIGNAL 1
OUTPUT SIGNAGL 1
CONTROL SIGNAL 2
OUTPUT SIGNAGL 2
CONTROL SIGNAL 3
OUTPUT SIGNAGL 3
SUPERPOSED
OUTPUT SIGNAL

Fig.19

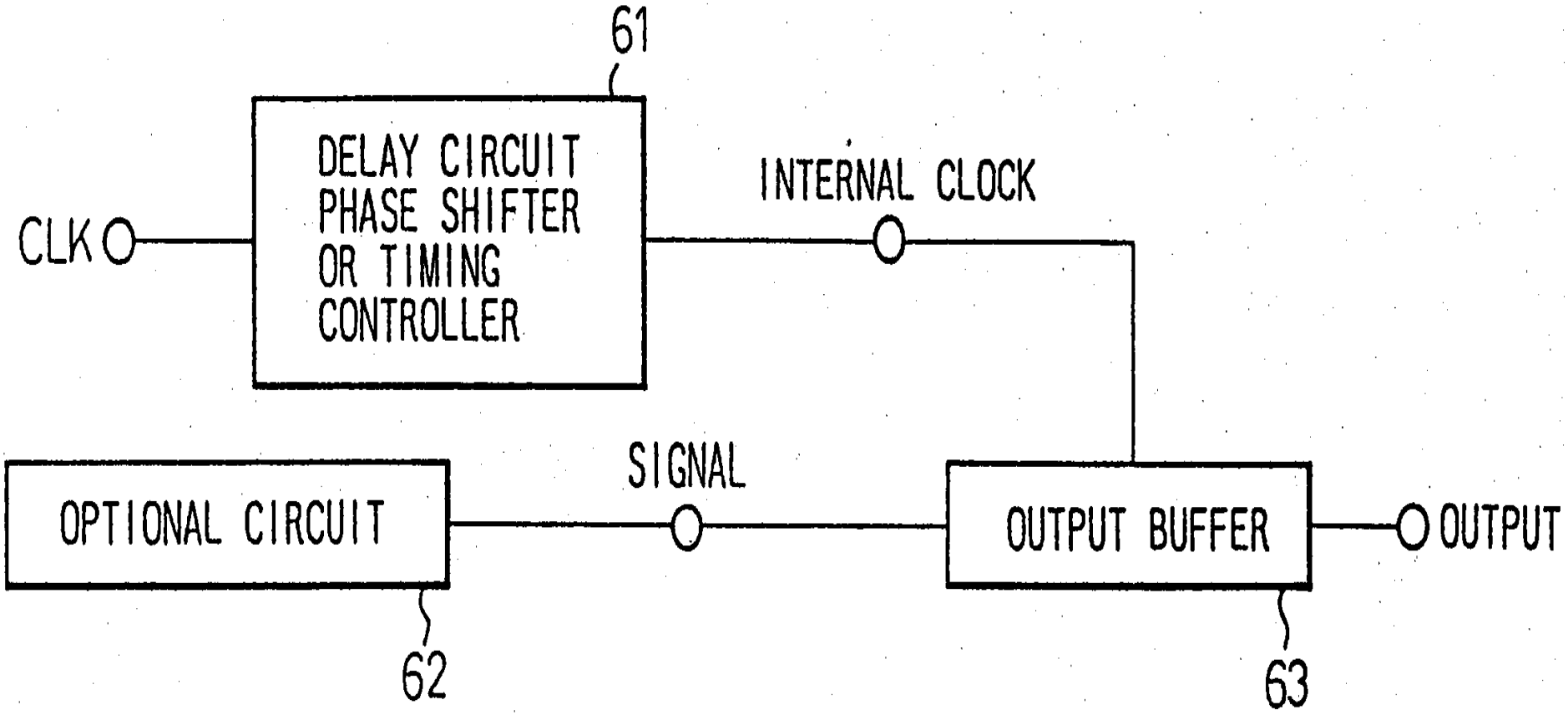

61
DELAY CIRCUIT
PHASE SHIFTER
OR TIMING
CONTROLLER
CLK
INTERNAL CLOCK
SIGNAL
OPTIONAL CIRCUIT
OUTPUT BUFFER
OUTPUT
62
63

Fig.20A

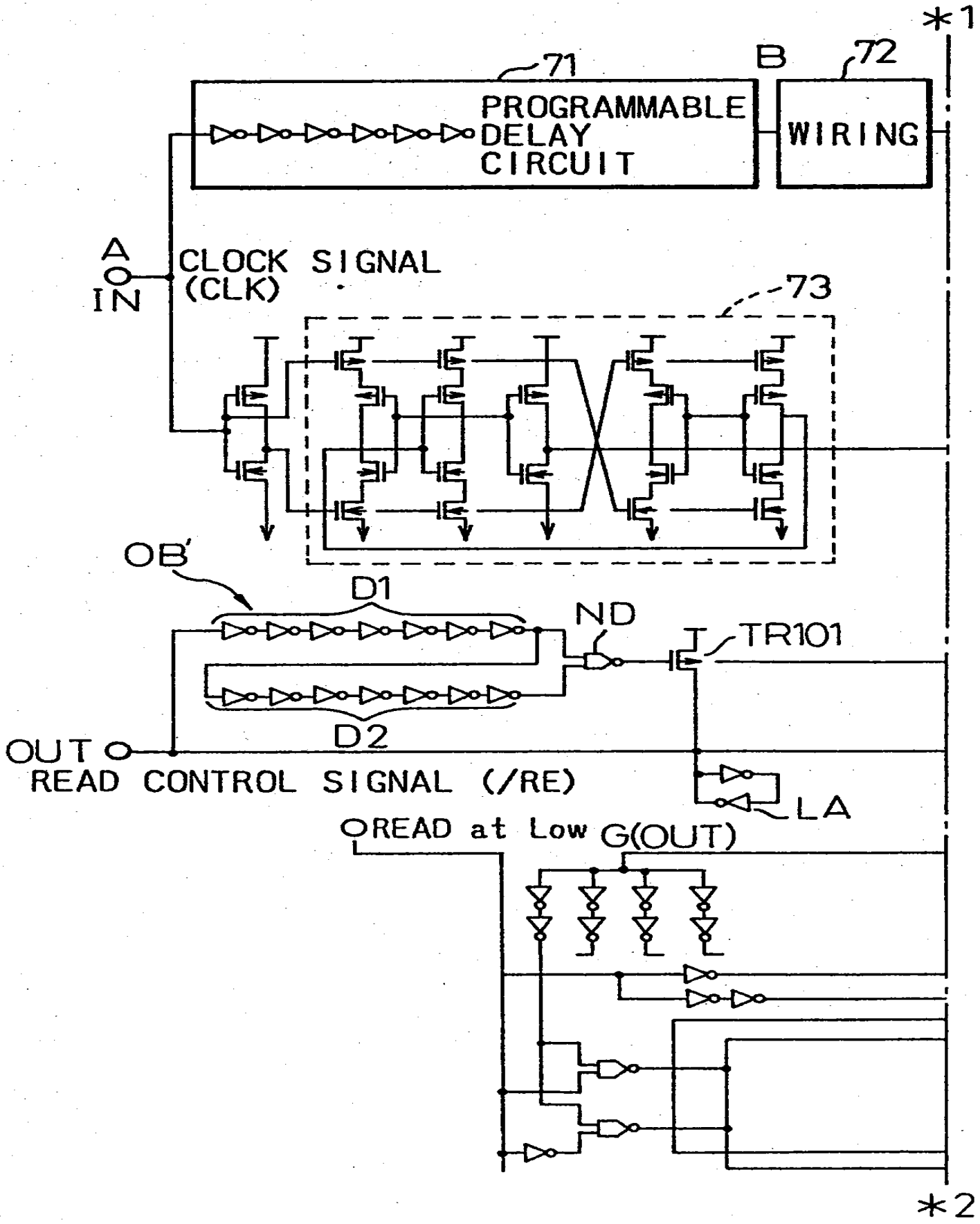

*1
71
B
72
PROGRAMMABLE DELAY CIRCUIT
WIRING
A
IN
CLOCK SIGNAL (CLK)
73
OB'
D1
ND
TR101
D2
OUT
READ CONTROL SIGNAL (/RE)
LA
READ at Low
G(OUT)
*2

Fig. 20B

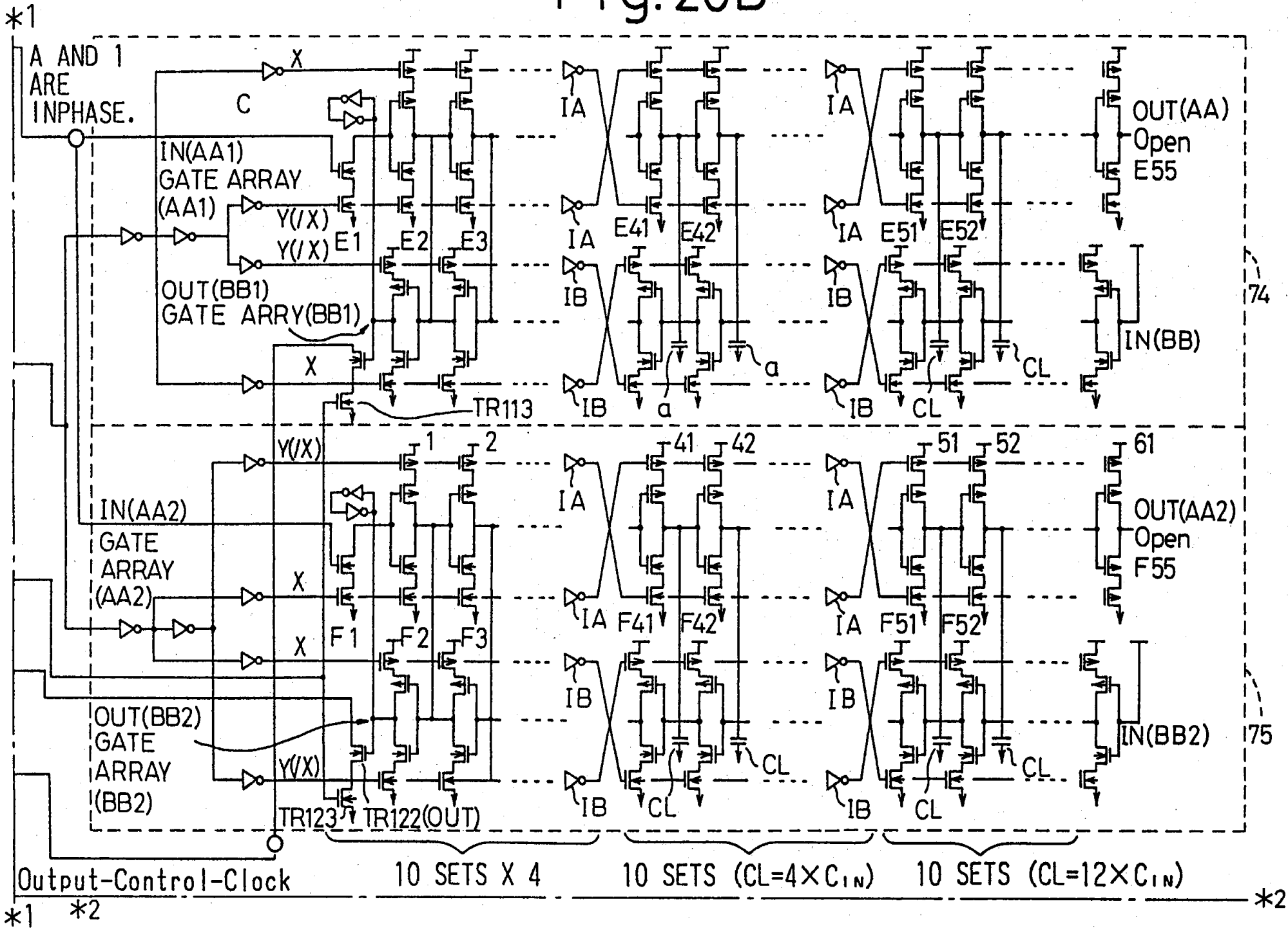

*1
A AND 1 ARE INPHASE.
X
C
IN(AA1) GATE ARRAY (AA1)
Y(/X)
Y(/X)
E1
E2
E3
OUT(BB1) GATE ARRY(BB1)
X
TR113
IA
IB
E41
E42
a
IA
IB
E51
E52
CL
OUT(AA) Open E55
IN(BB)
74
Y(/X)
1
2
IN(AA2) GATE ARRAY (AA2)
X
X
F1
F2
F3
OUT(BB2) GATE ARRAY (BB2)
Y(/X)
TR123
TR122(OUT)
41
42
F41
F42
51
52
F51
F52
61
OUT(AA2) Open F55
IN(BB2)
75
Output-Control-Clock
10 SETS X 4
10 SETS (CL=4×C_IN)
10 SETS (CL=12×C_IN)
*2

Fig. 20C

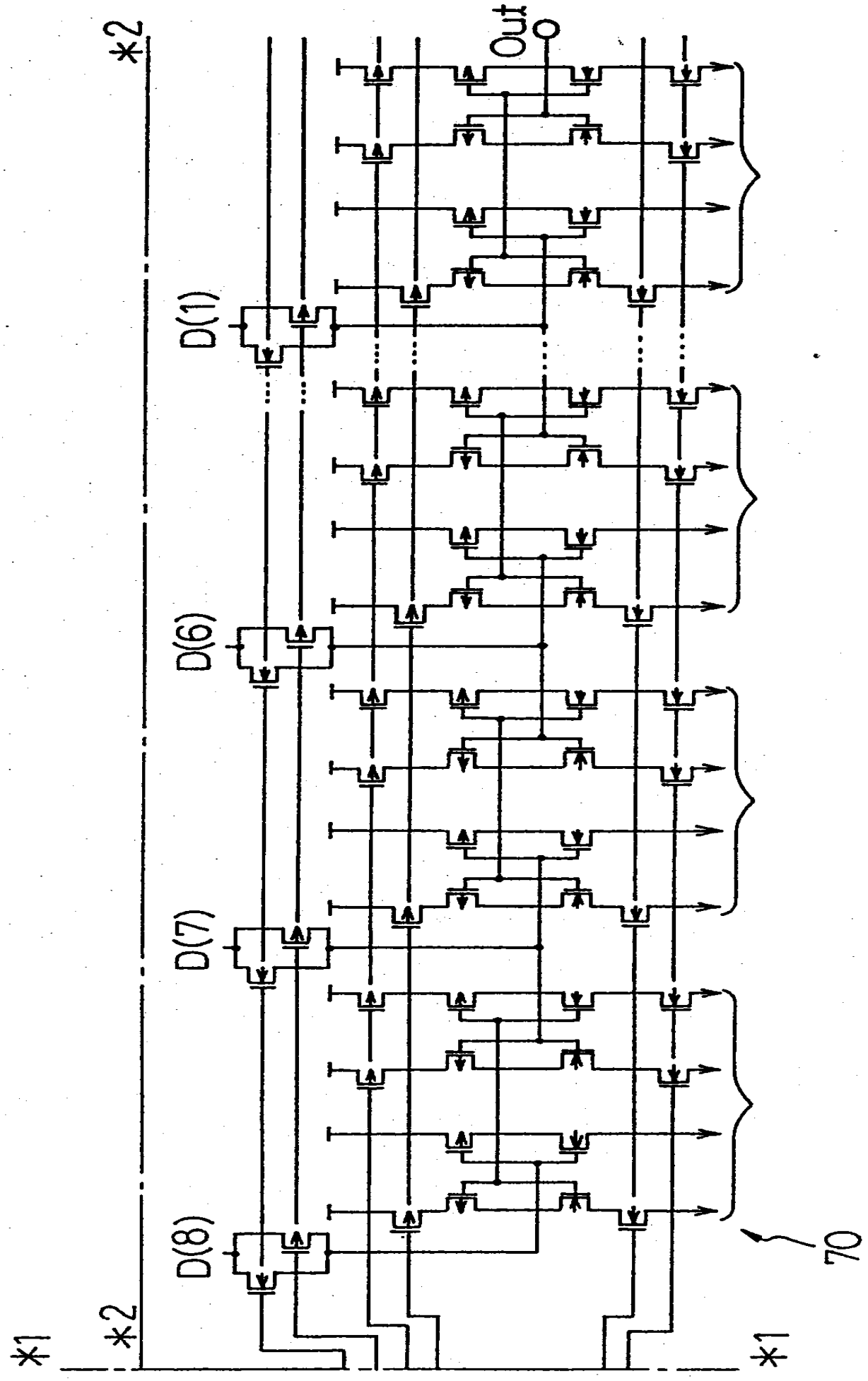


Fig.21A

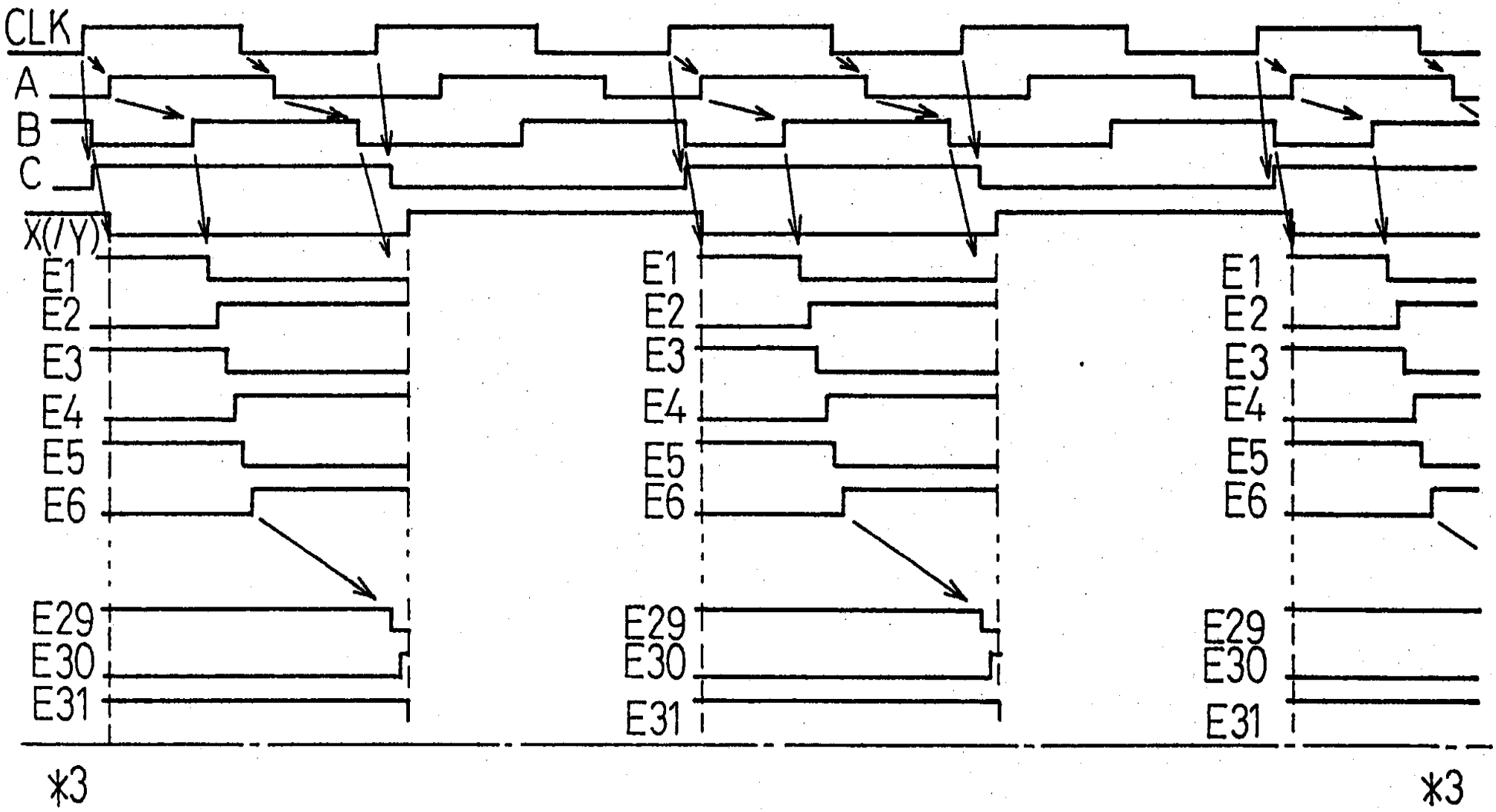

CLK
A
B
C
X(/Y)
E1
E2
E3
E4
E5
E6
E29
E30
E31
*3
E1
E2
E3
E4
E5
E6
E29
E30
E31
E1
E2
E3
E4
E5
E6
E29
E30
E31
*3

Fig.21B

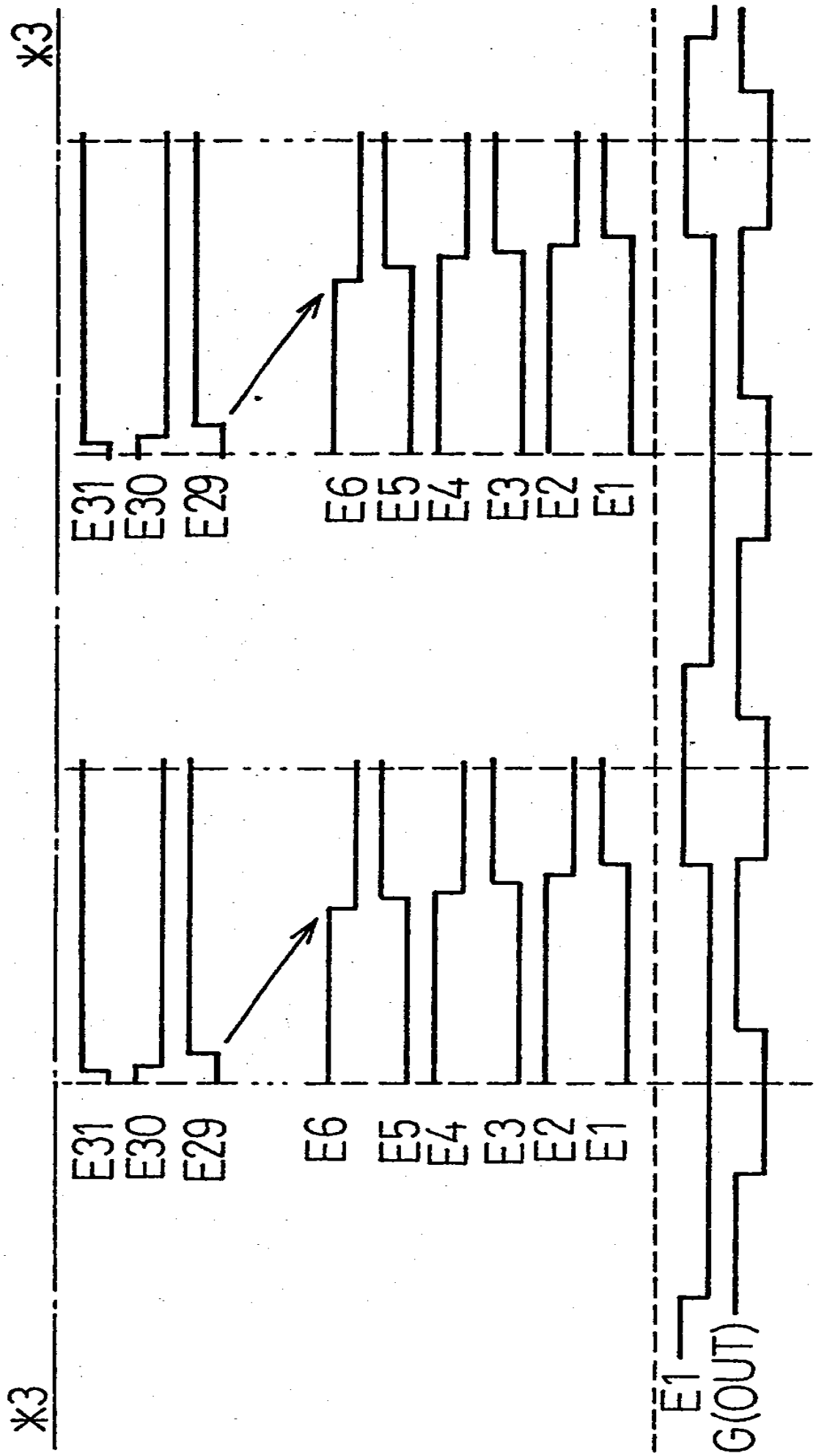

×3
E31
E30
E29
E6
E5
E4
E3
E2
E1
E31
E30
E29
E6
E5
E4
E3
E2
E1
×3
E1
G(OUT)

Fig.22

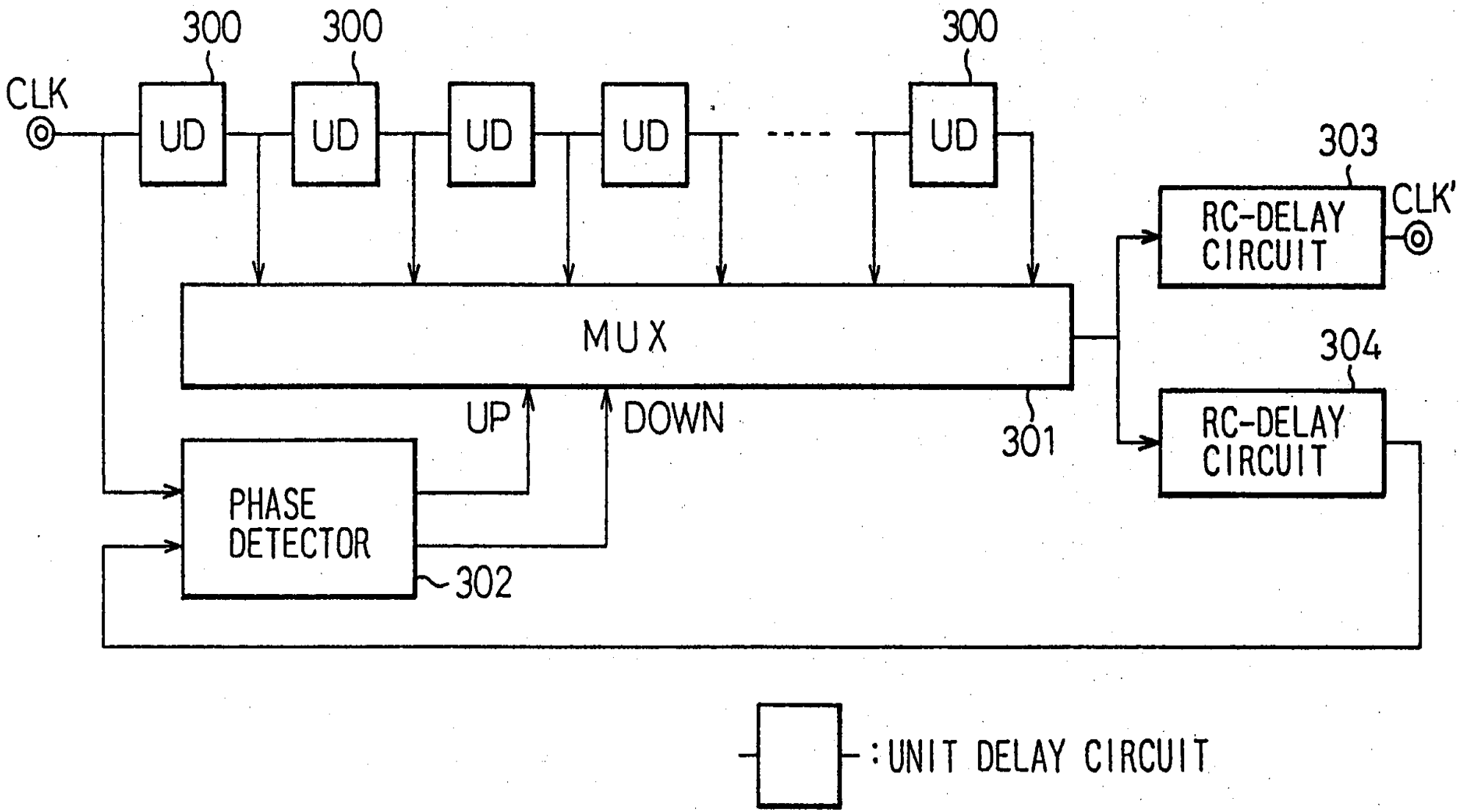

300
300
300
CLK
UD
UD
UD
UD
UD
303
RC-DELAY CIRCUIT
CLK'
MUX
304
RC-DELAY CIRCUIT
UP
DOWN
301
PHASE DETECTOR
302
: UNIT DELAY CIRCUIT

Fig. 23

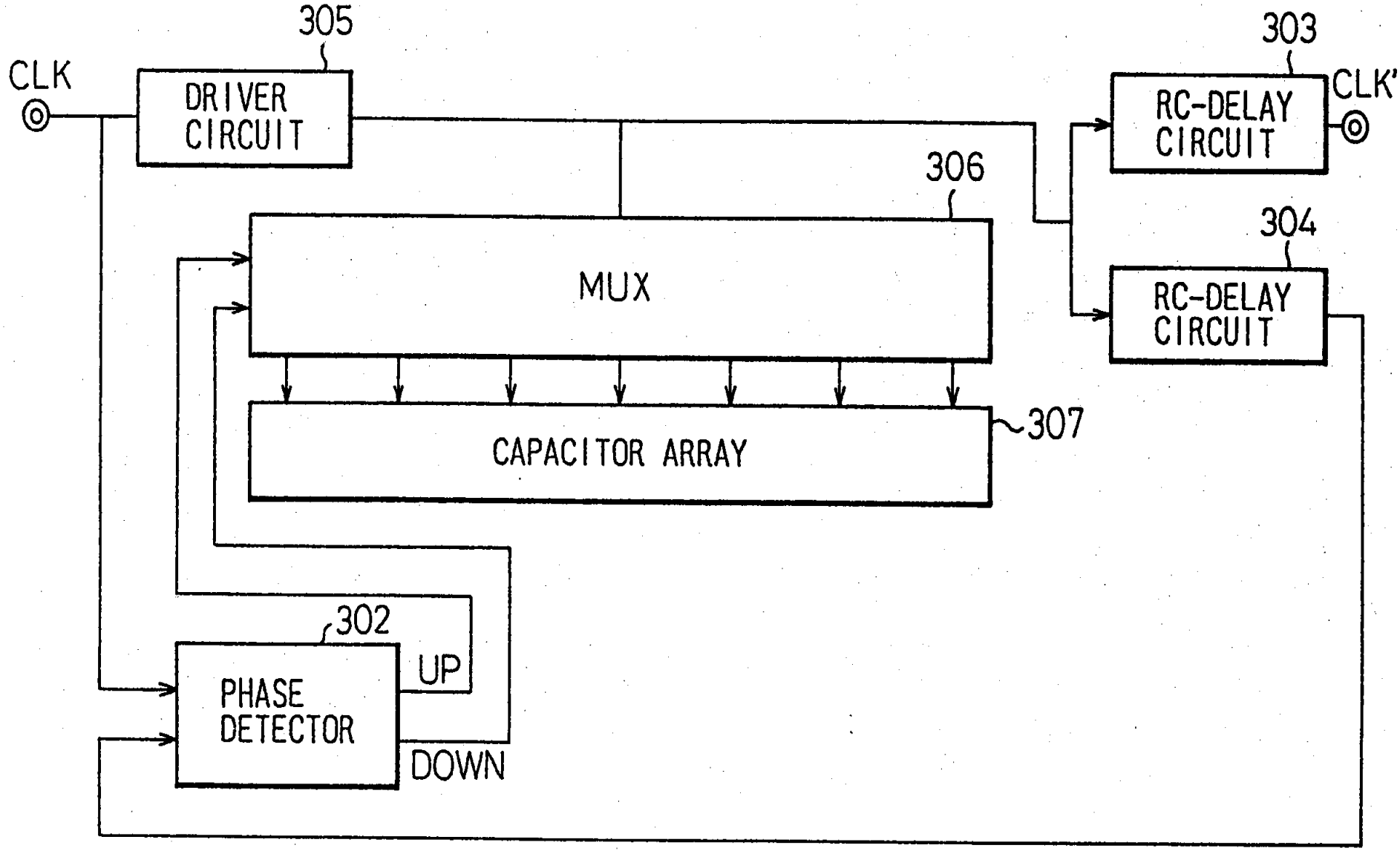

CLK
305
DRIVER CIRCUIT
303
RC-DELAY CIRCUIT
CLK'
306
MUX
304
RC-DELAY CIRCUIT
CAPACITOR ARRAY
307
302
PHASE DETECTOR
UP
DOWN

Fig. 24

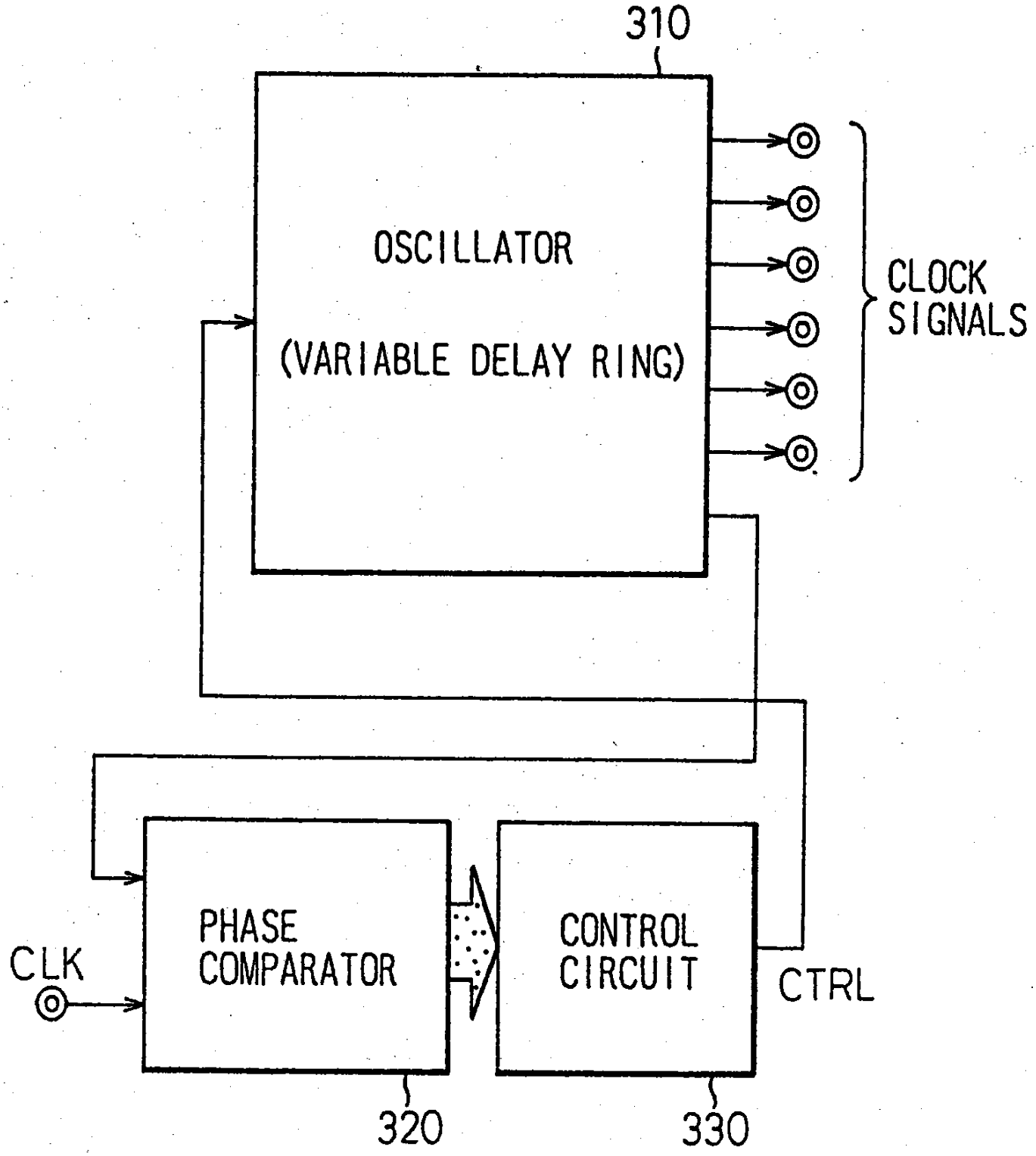

310
OSCILLATOR
(VARIABLE DELAY RING)
CLOCK SIGNALS
CLK
PHASE COMPARATOR
CONTROL CIRCUIT
CTRL
320
330

Fig. 25

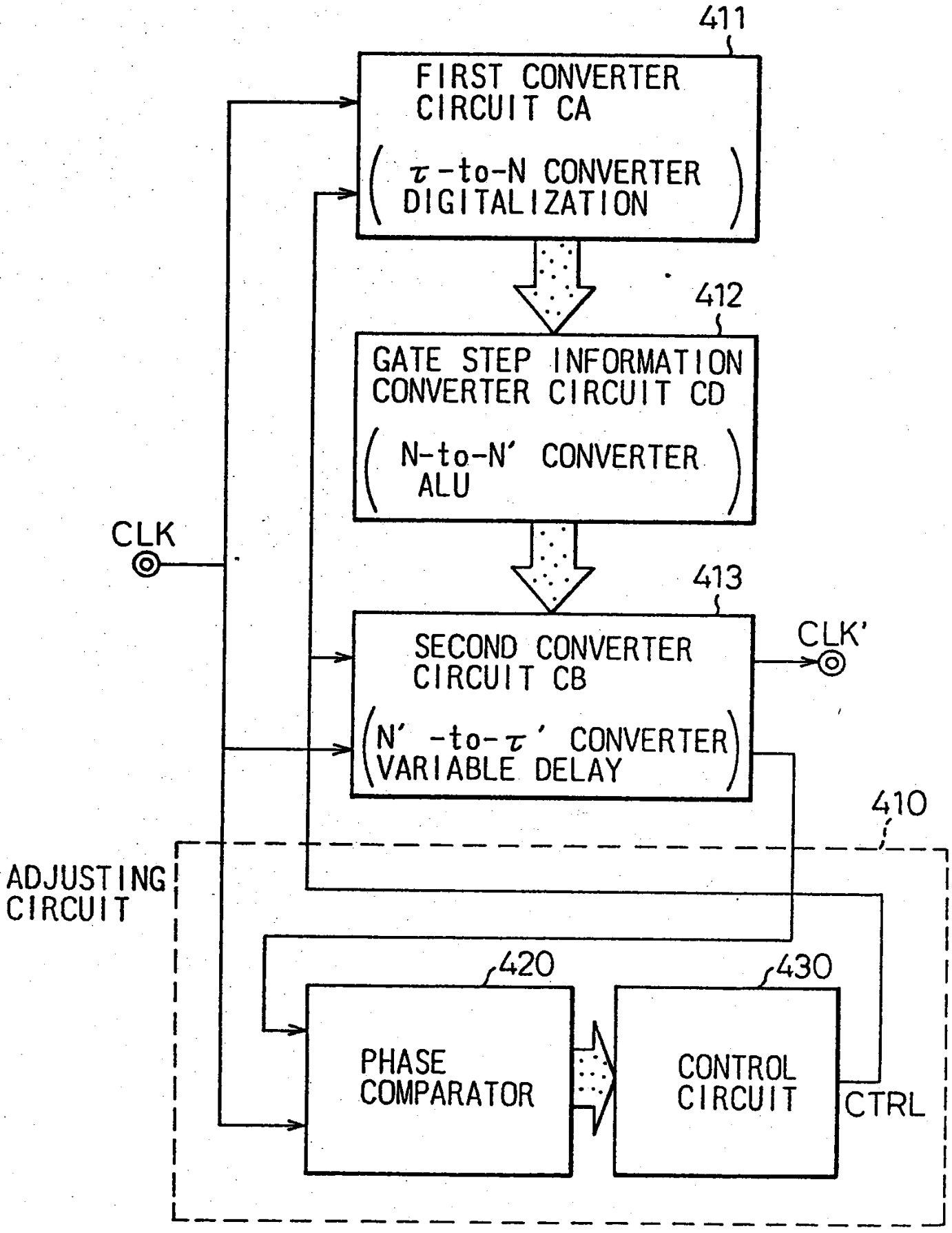

411
FIRST CONVERTER CIRCUIT CA
(τ-to-N CONVERTER DIGITALIZATION)
412
GATE STEP INFORMATION CONVERTER CIRCUIT CD
(N-to-N' CONVERTER ALU)
CLK
413
SECOND CONVERTER CIRCUIT CB
(N'-to-τ' CONVERTER VARIABLE DELAY)
CLK'
410
ADJUSTING CIRCUIT
420
PHASE COMPARATOR
430
CONTROL CIRCUIT
CTRL

Fig. 26A

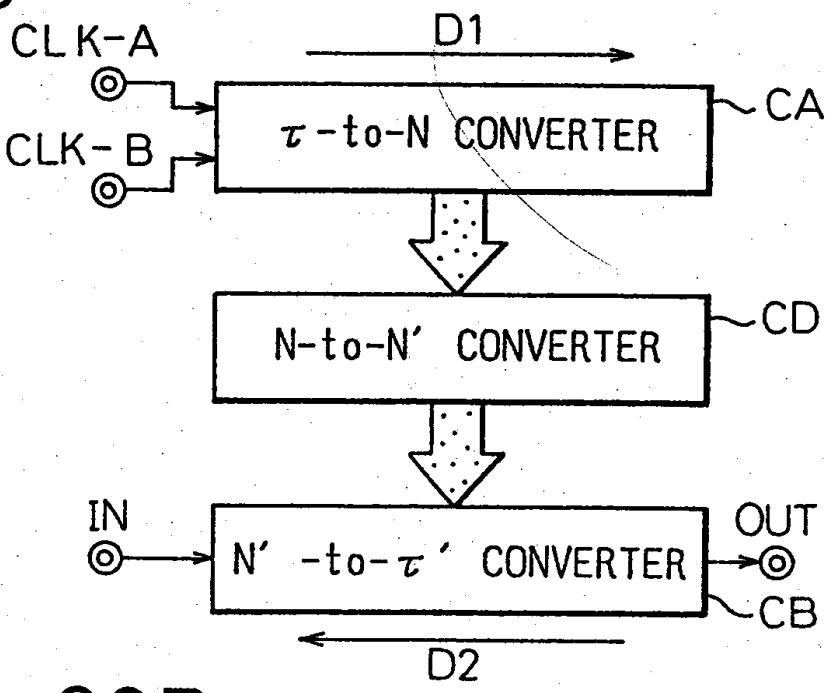


Fig. 26B

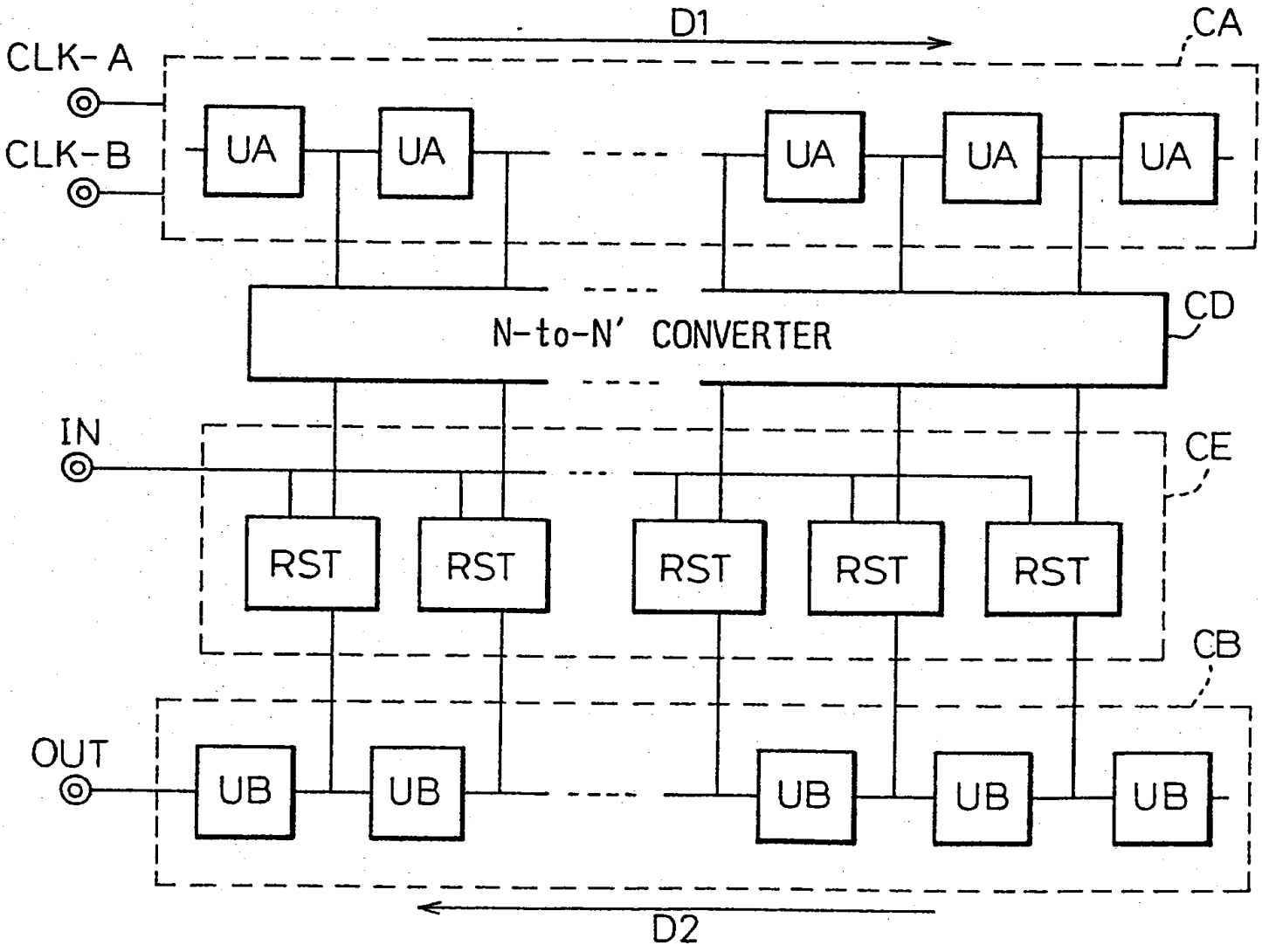


Fig.27A

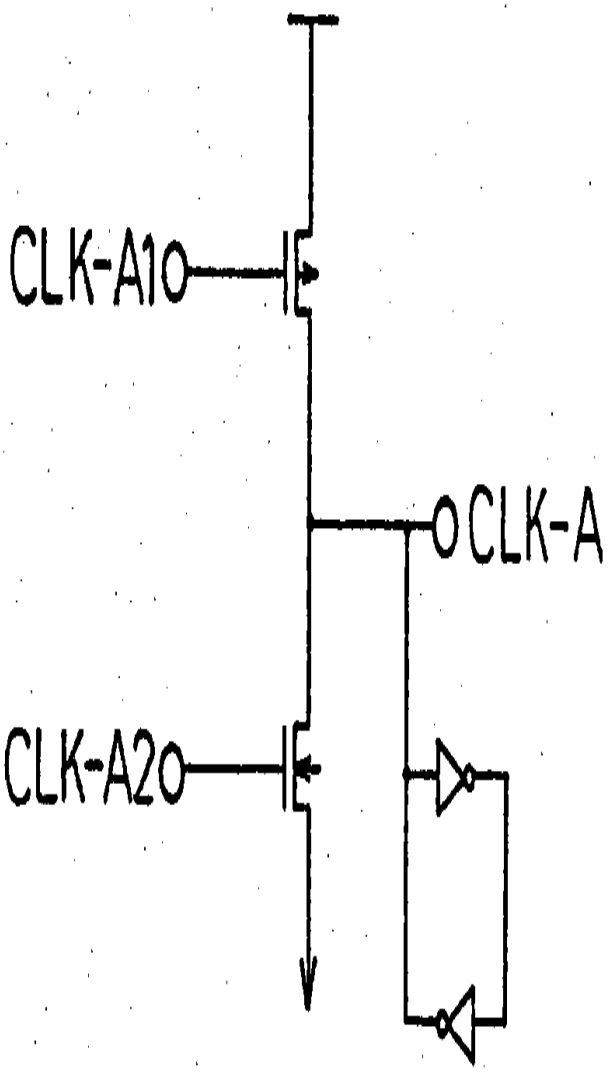


Fig.27B

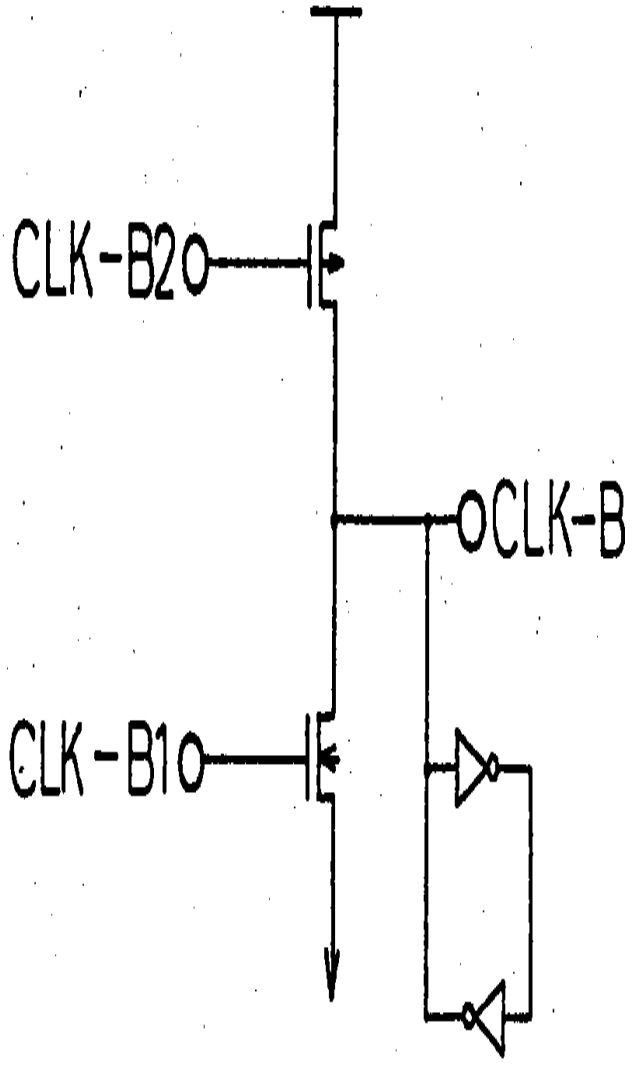


Fig.27C

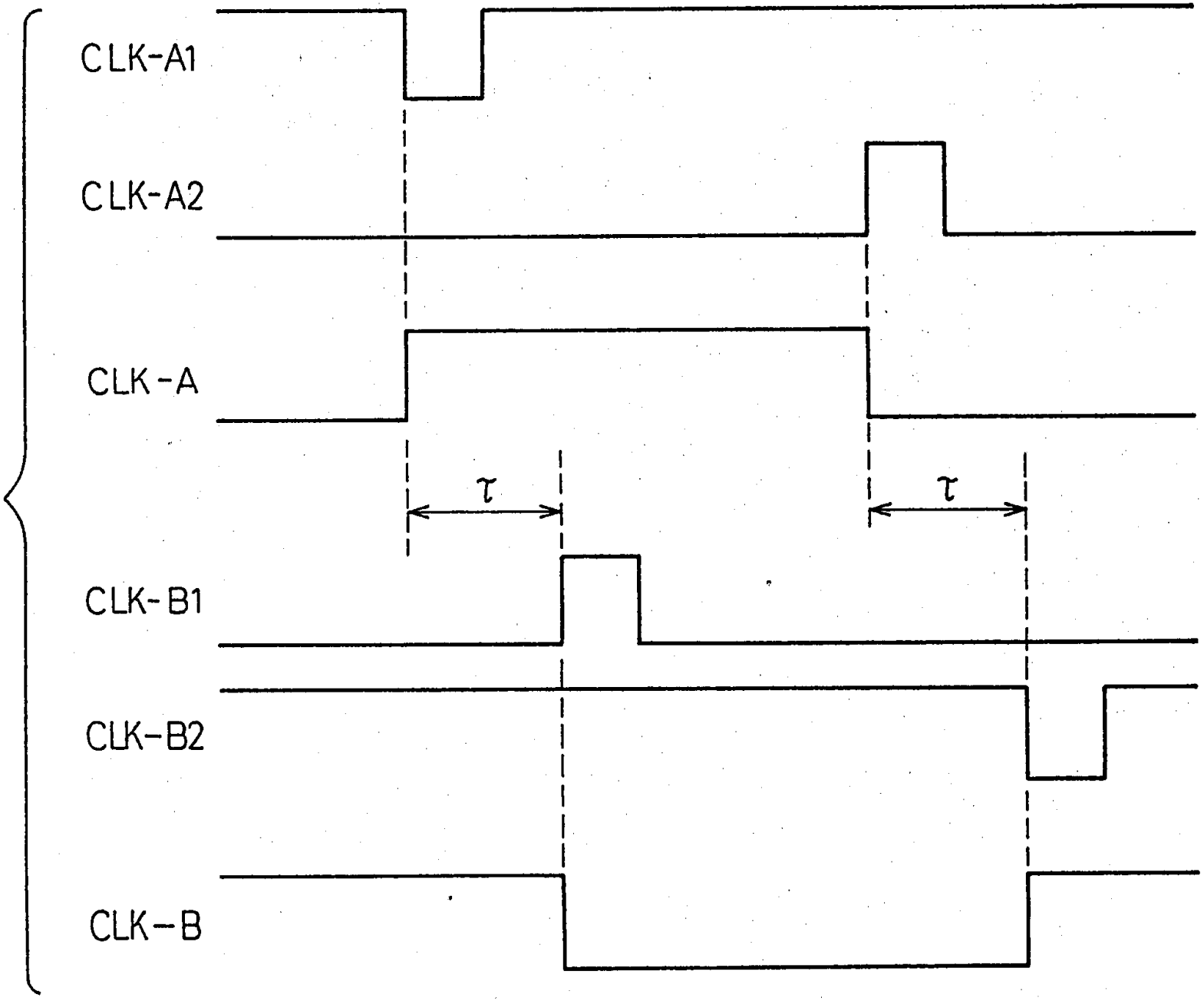


Fig. 28

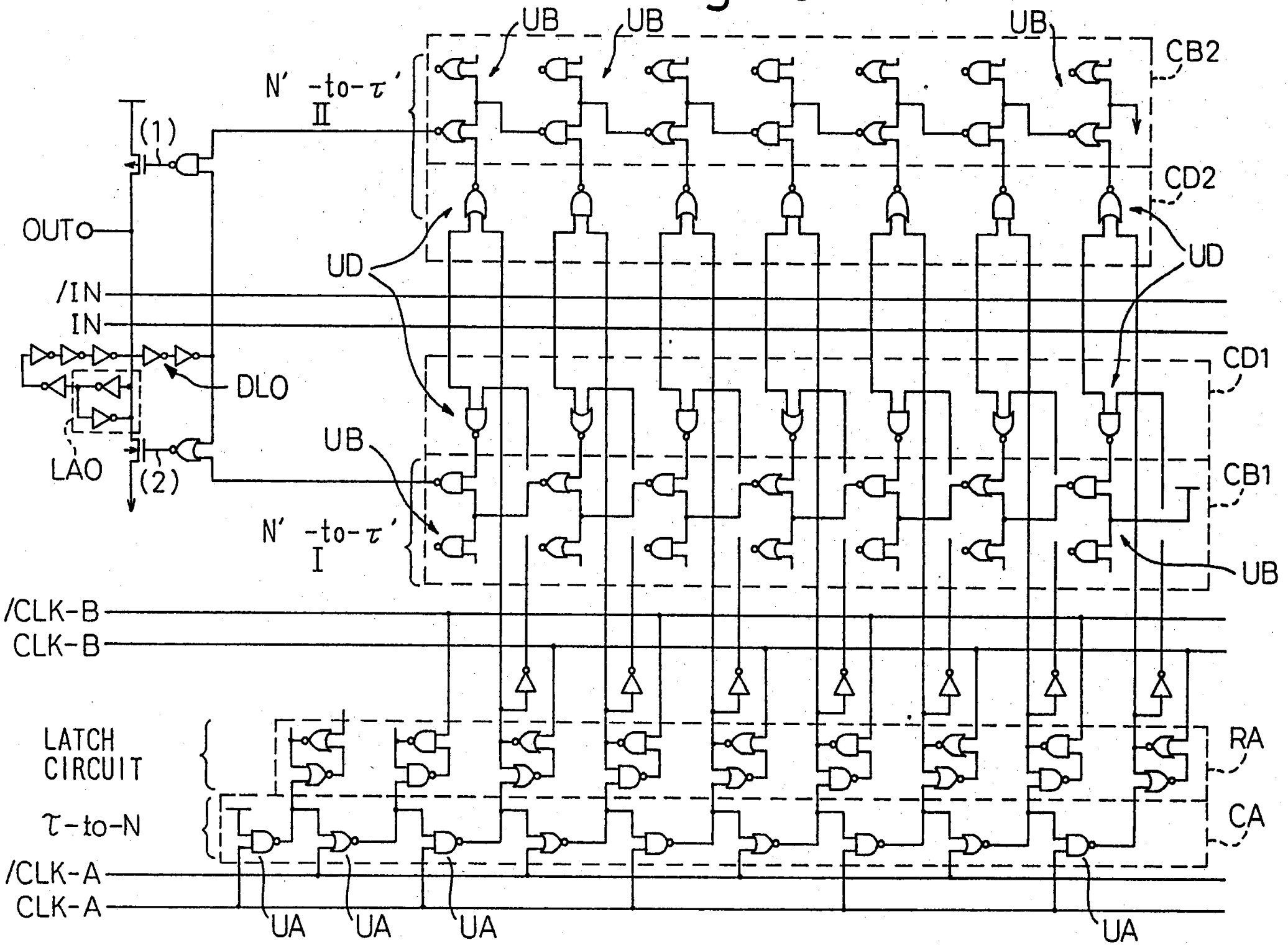

UB
UB
UB
CB2
N' -to-τ'
II
(1)
CD2
OUTo
UD
UD
/IN
IN
CD1
DLO
UB
LAO
(2)
CB1
N' -to-τ'
I
UB
/CLK-B
CLK-B
LATCH
CIRCUIT
RA
τ-to-N
CA
/CLK-A
CLK-A
UA
UA
UA
UA

Fig. 29

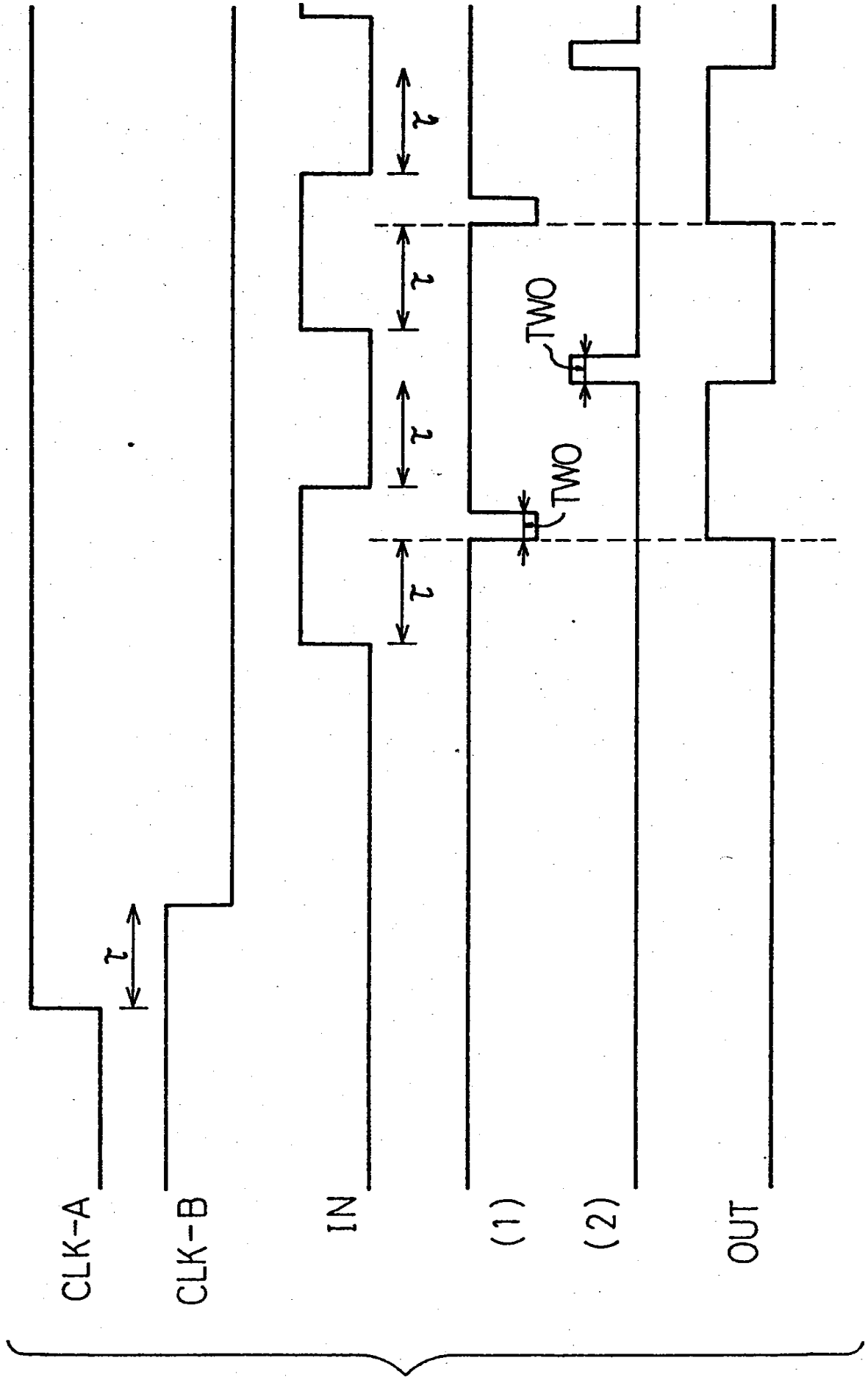


Fig. 30A

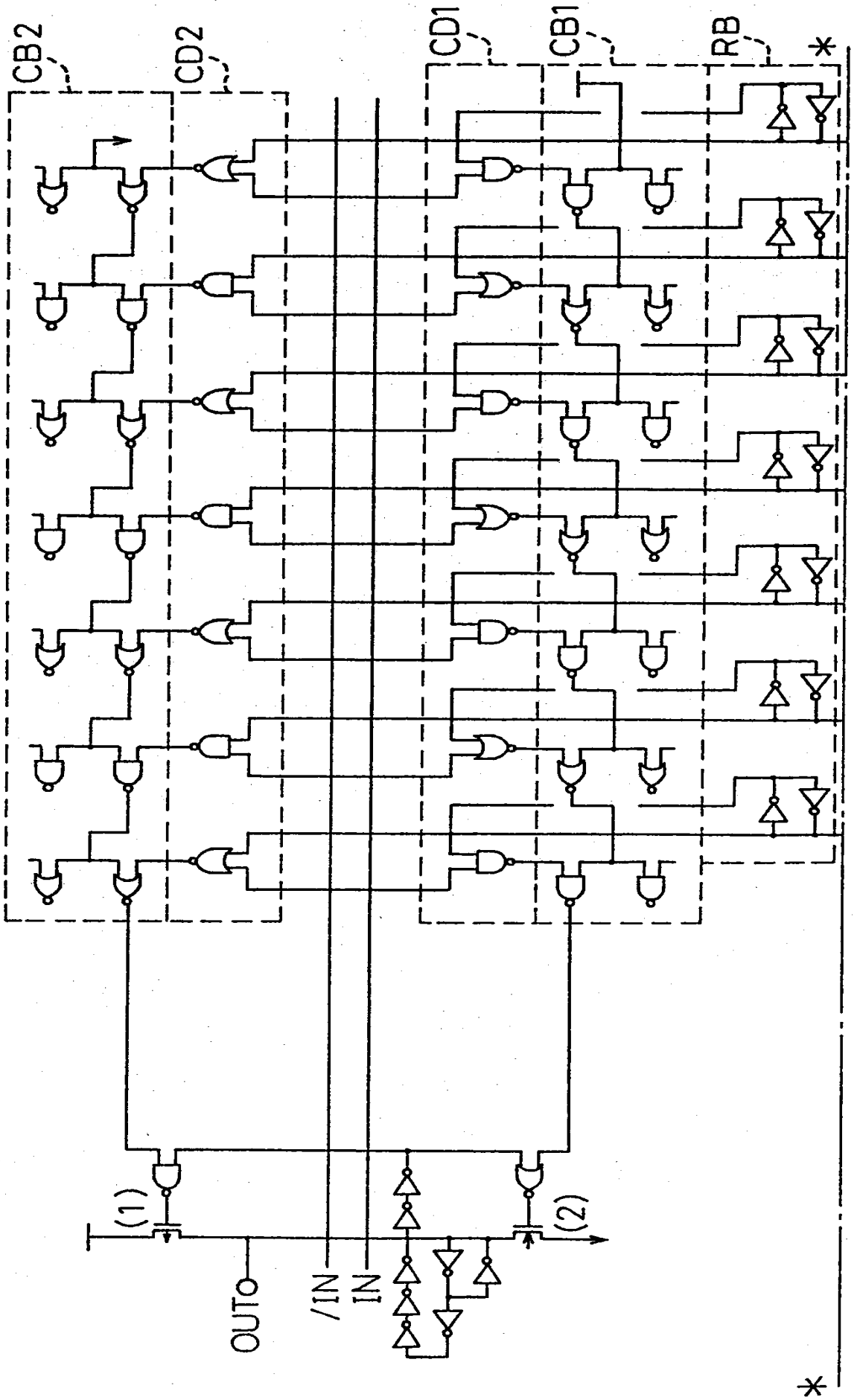


Fig. 30B

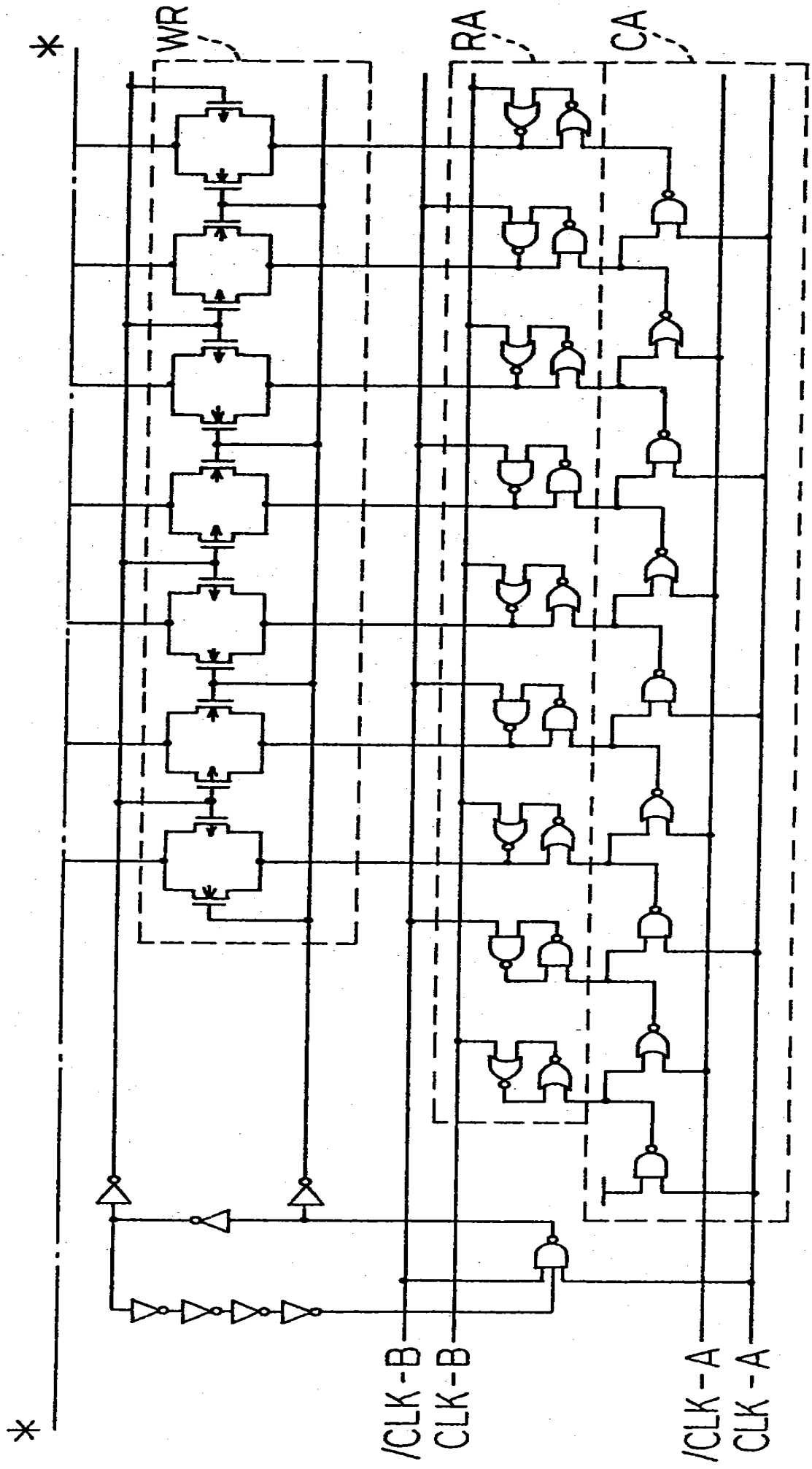


Fig.31

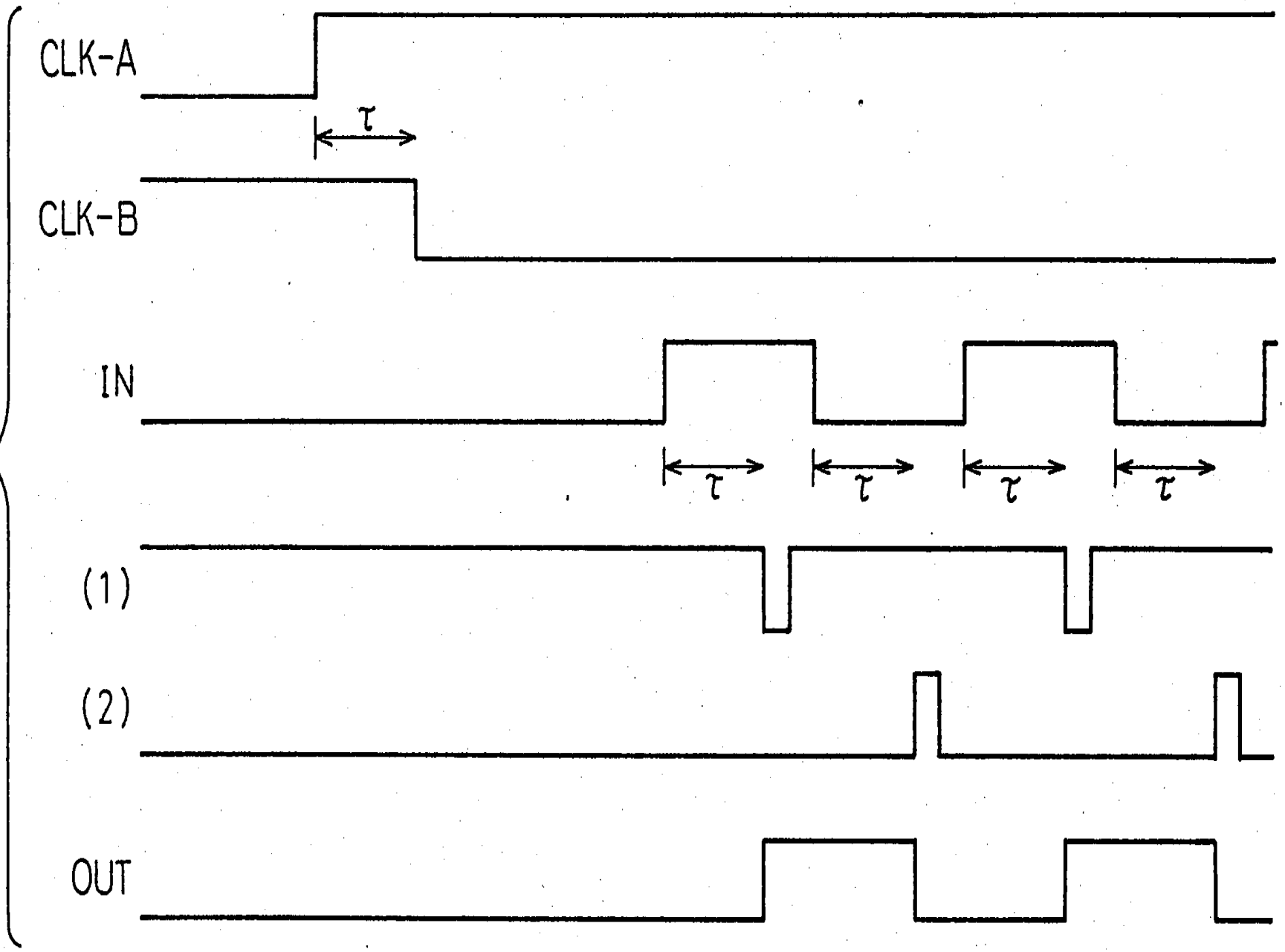


Fig. 32A

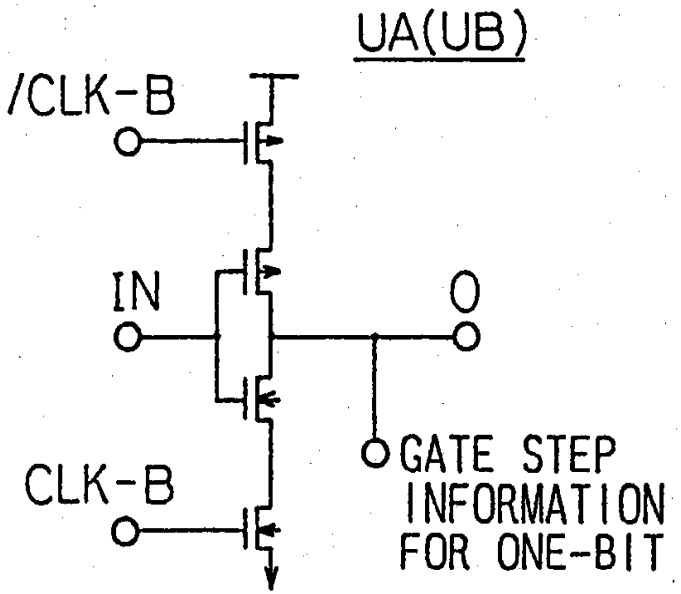


Fig. 32B

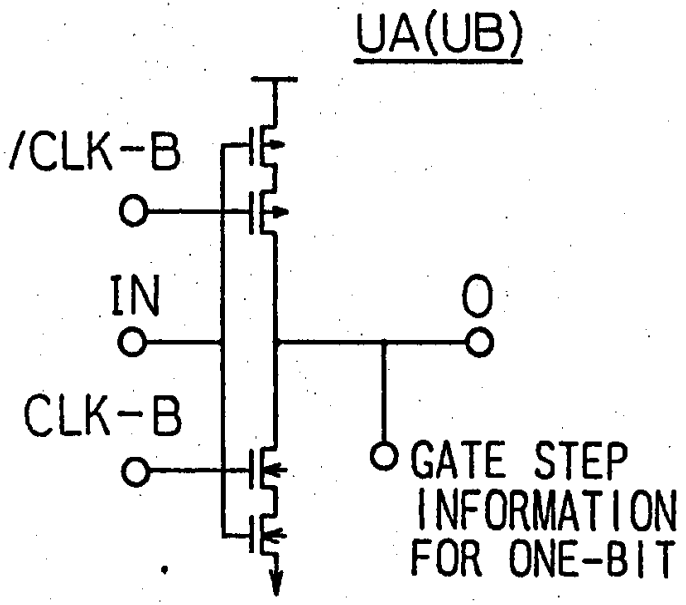


Fig. 32C

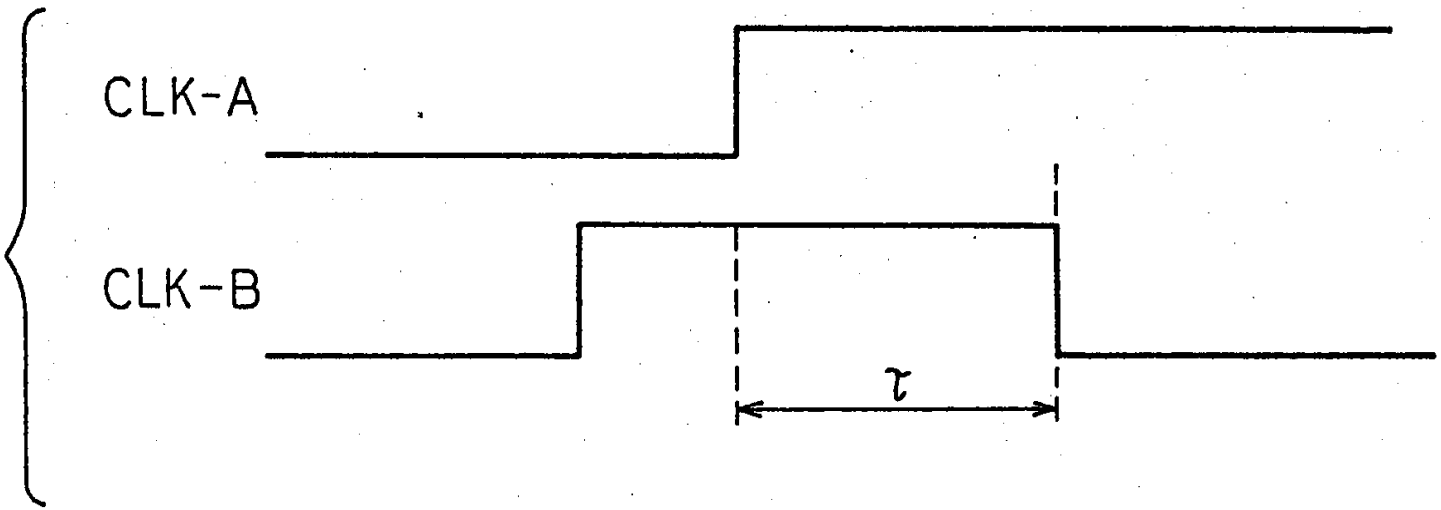


Fig.33A

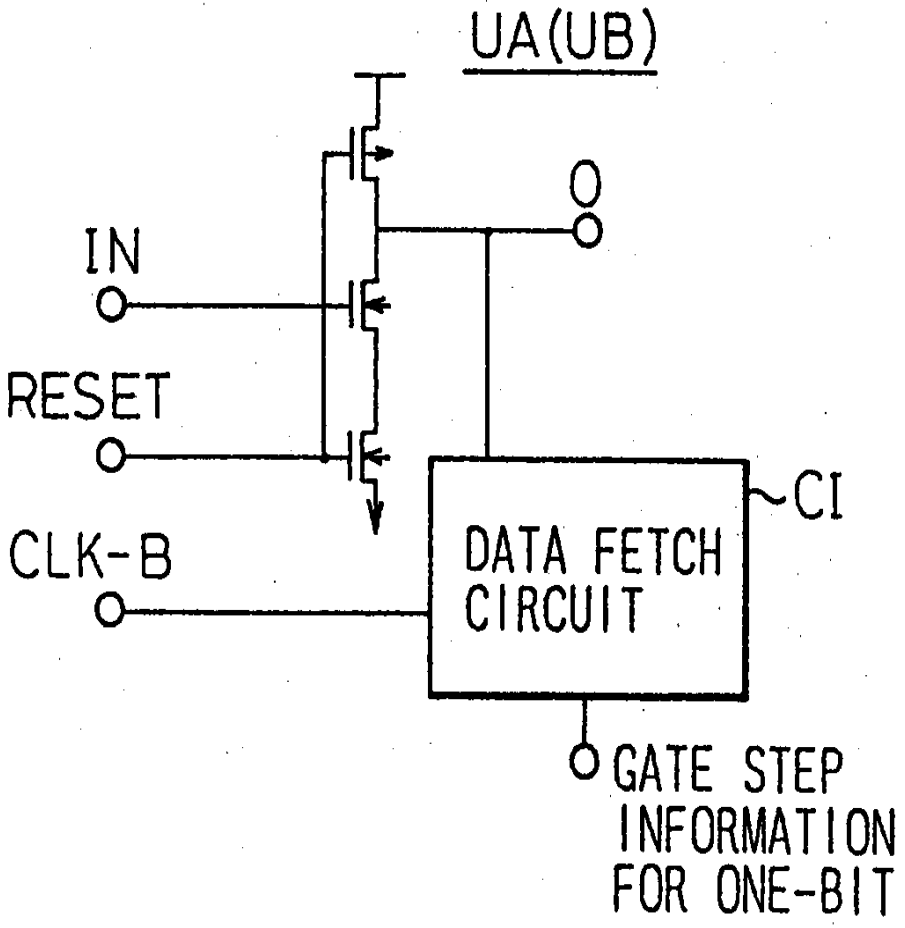


Fig.33B

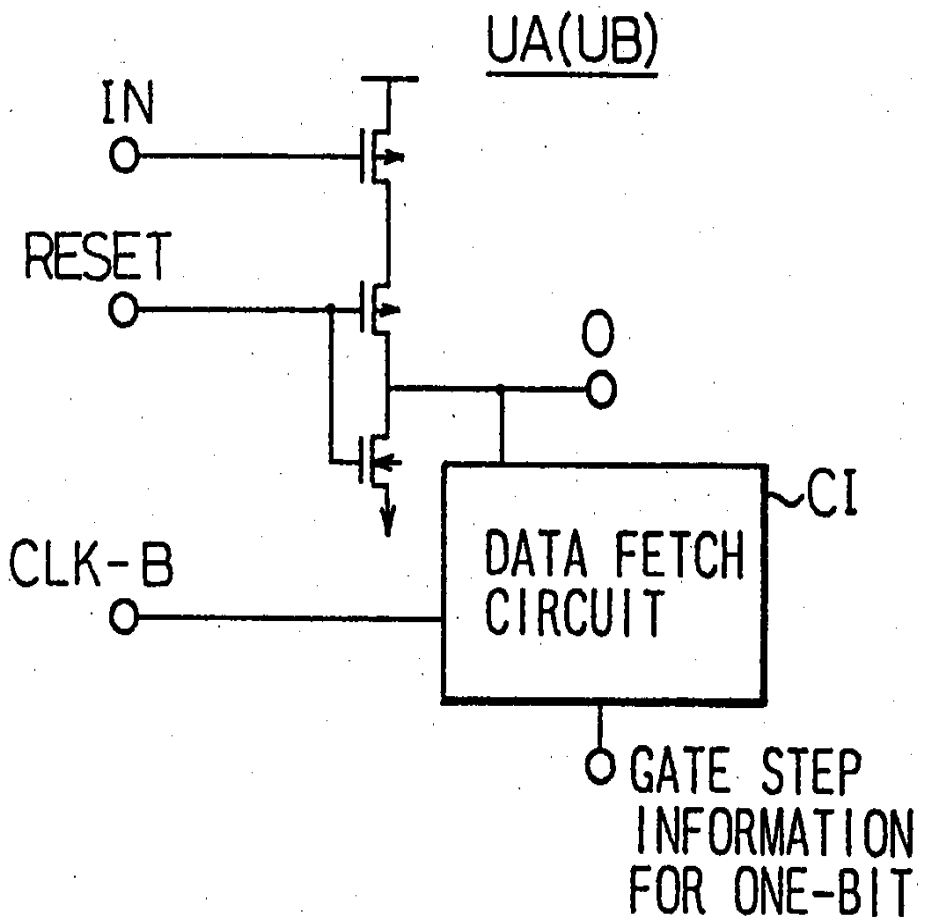


Fig.34A

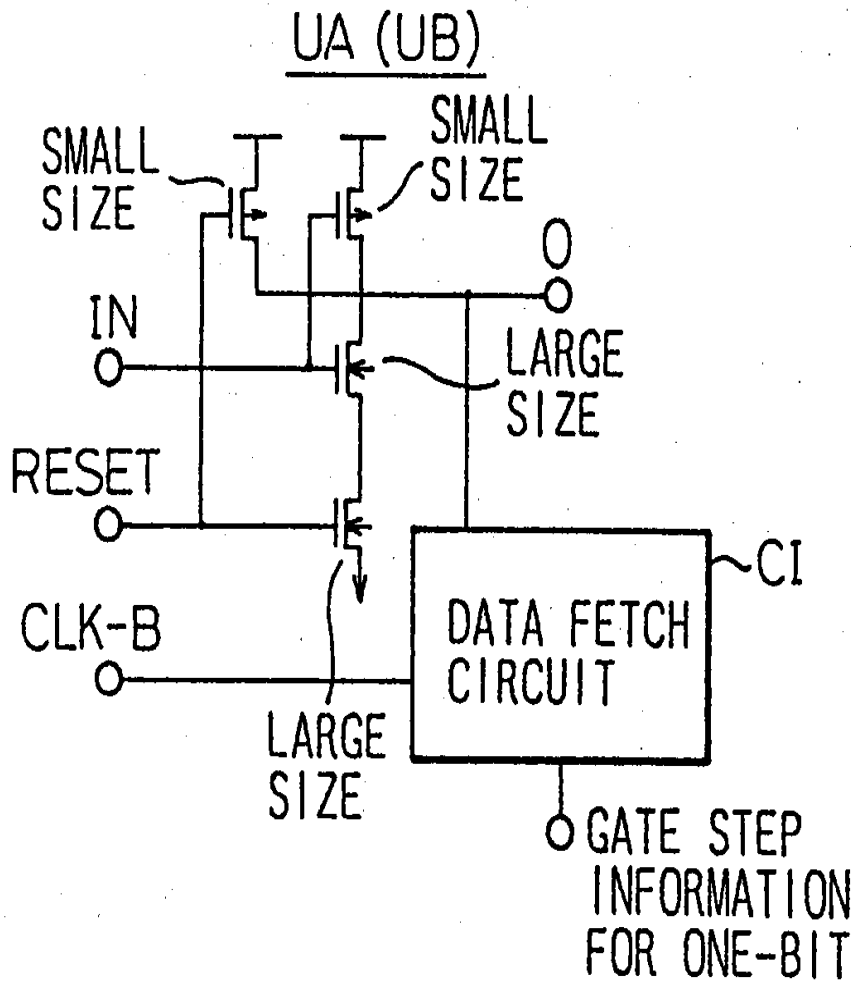


Fig.34B

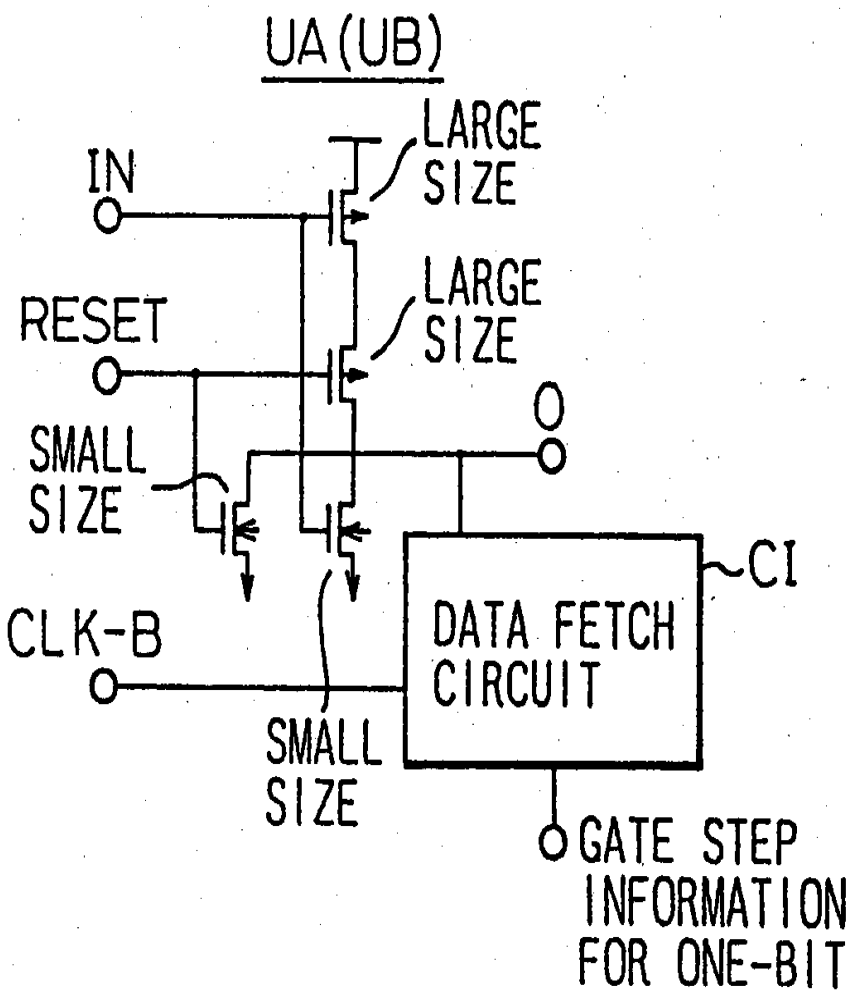


Fig. 35A

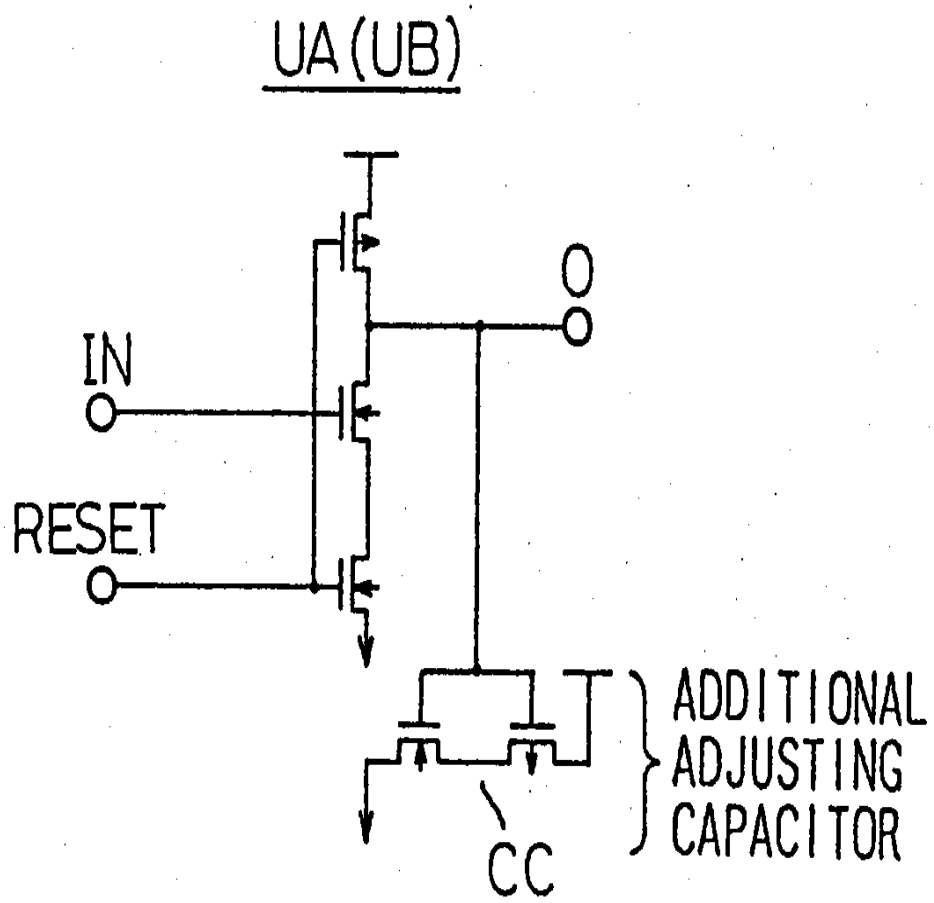


Fig. 35B

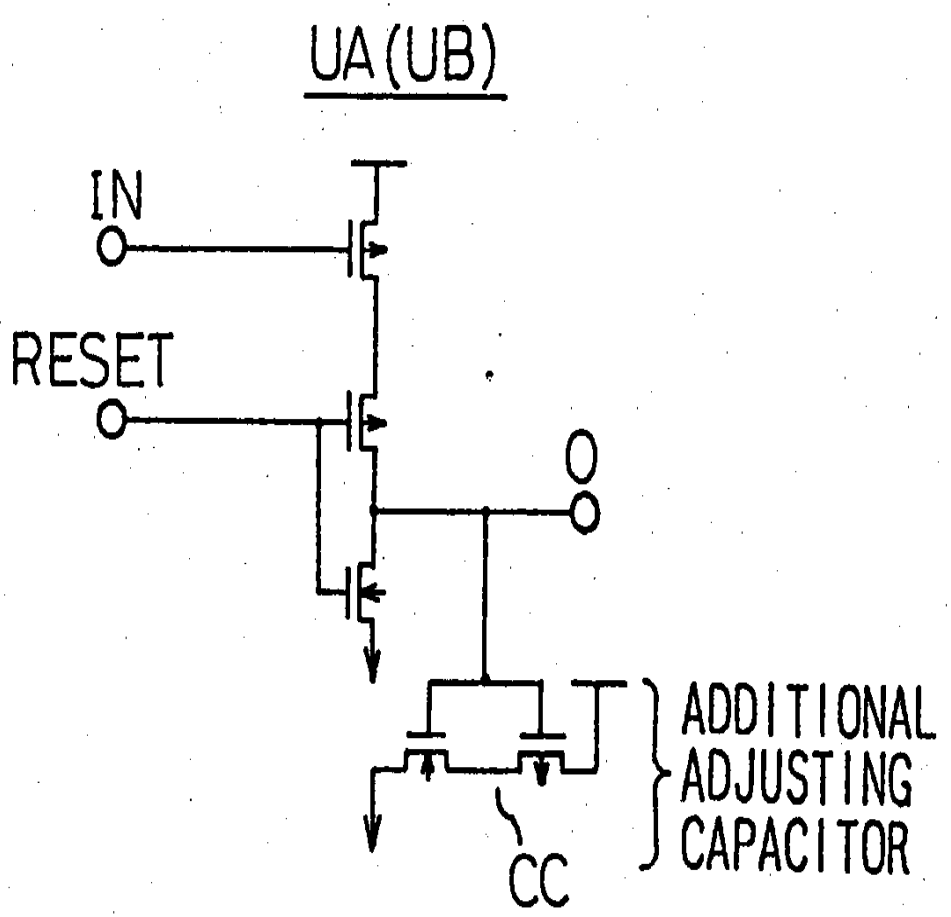


Fig.36

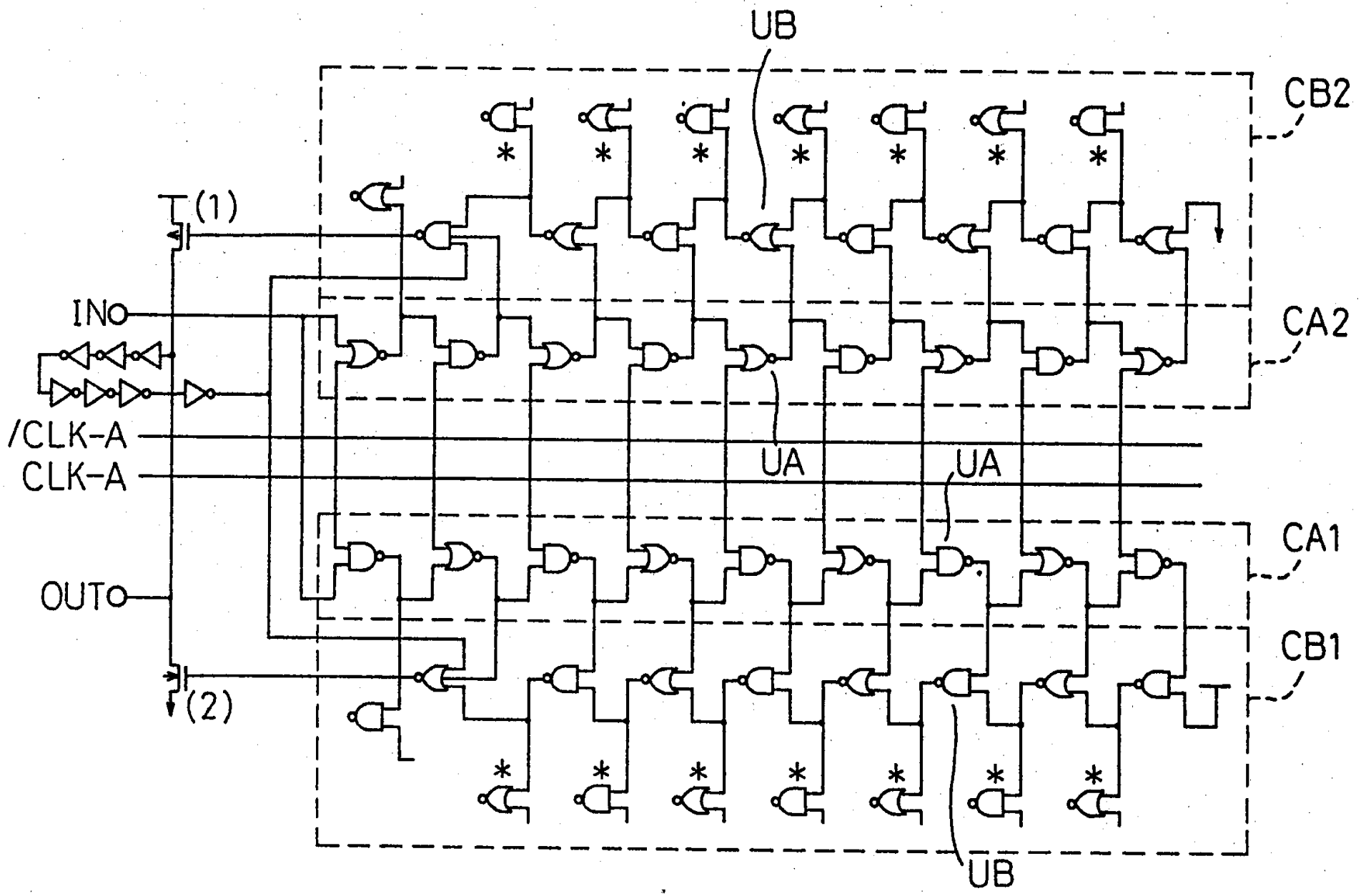


Fig. 37

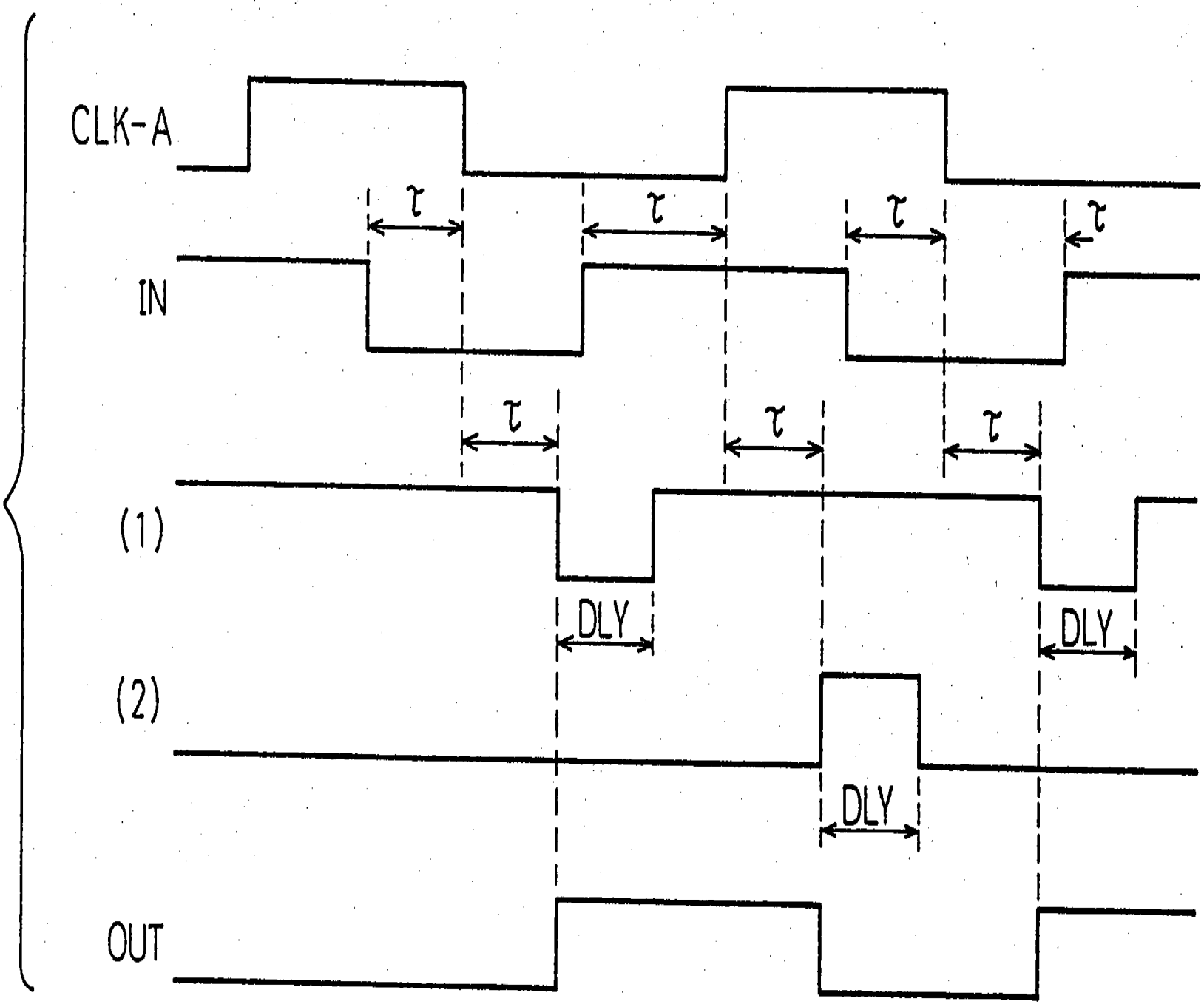


Fig. 38A

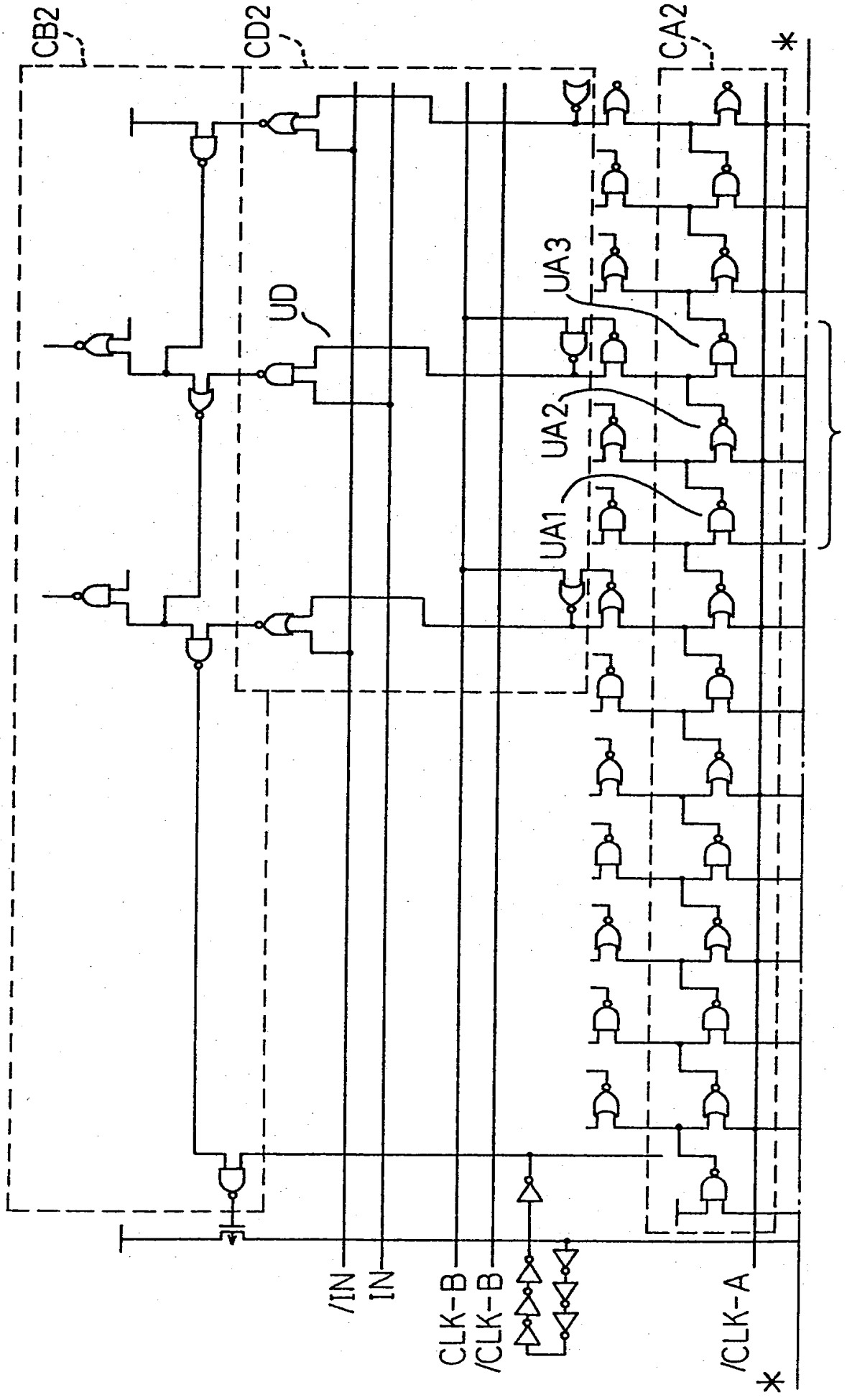


Fig. 38B

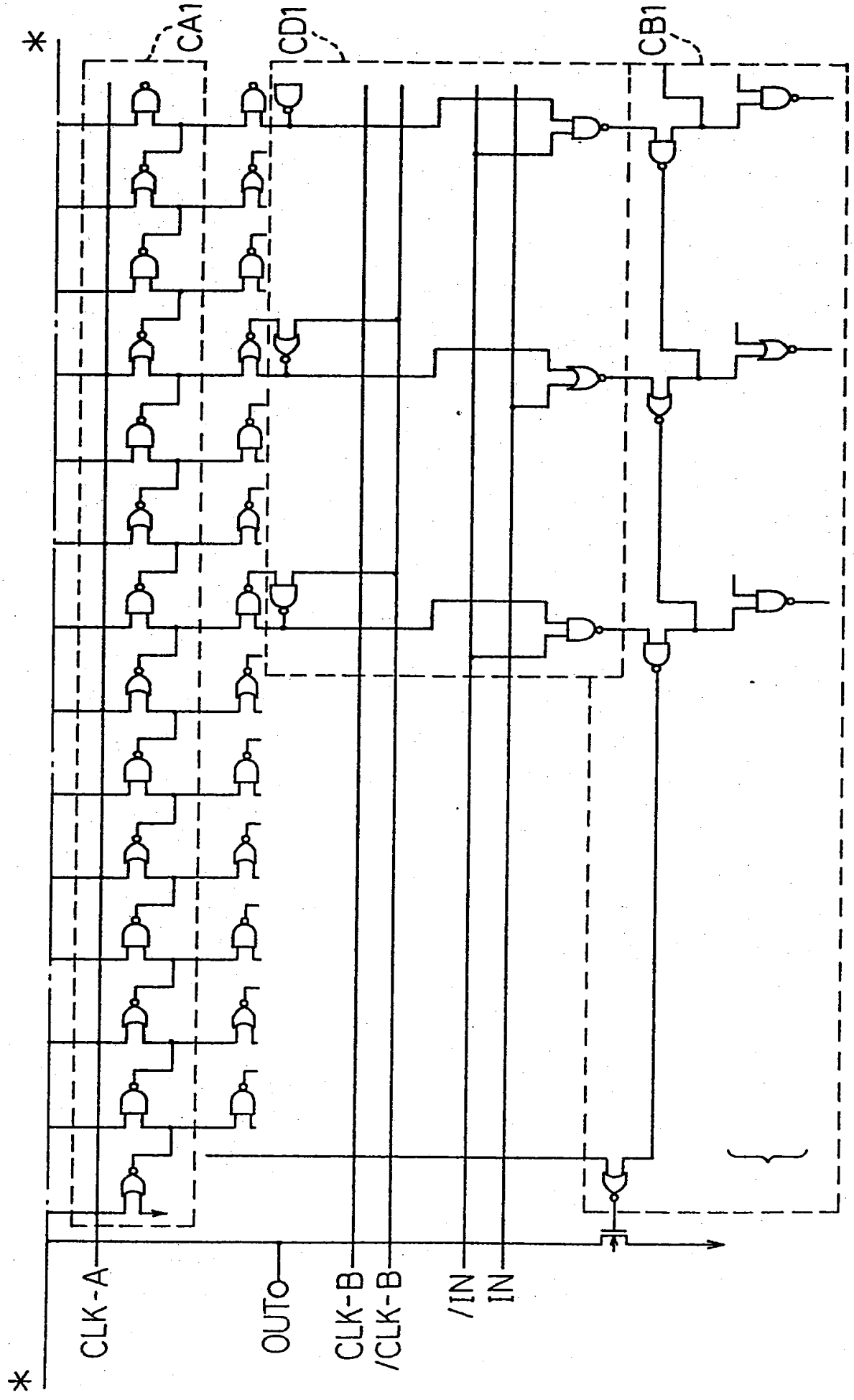


Fig. 39

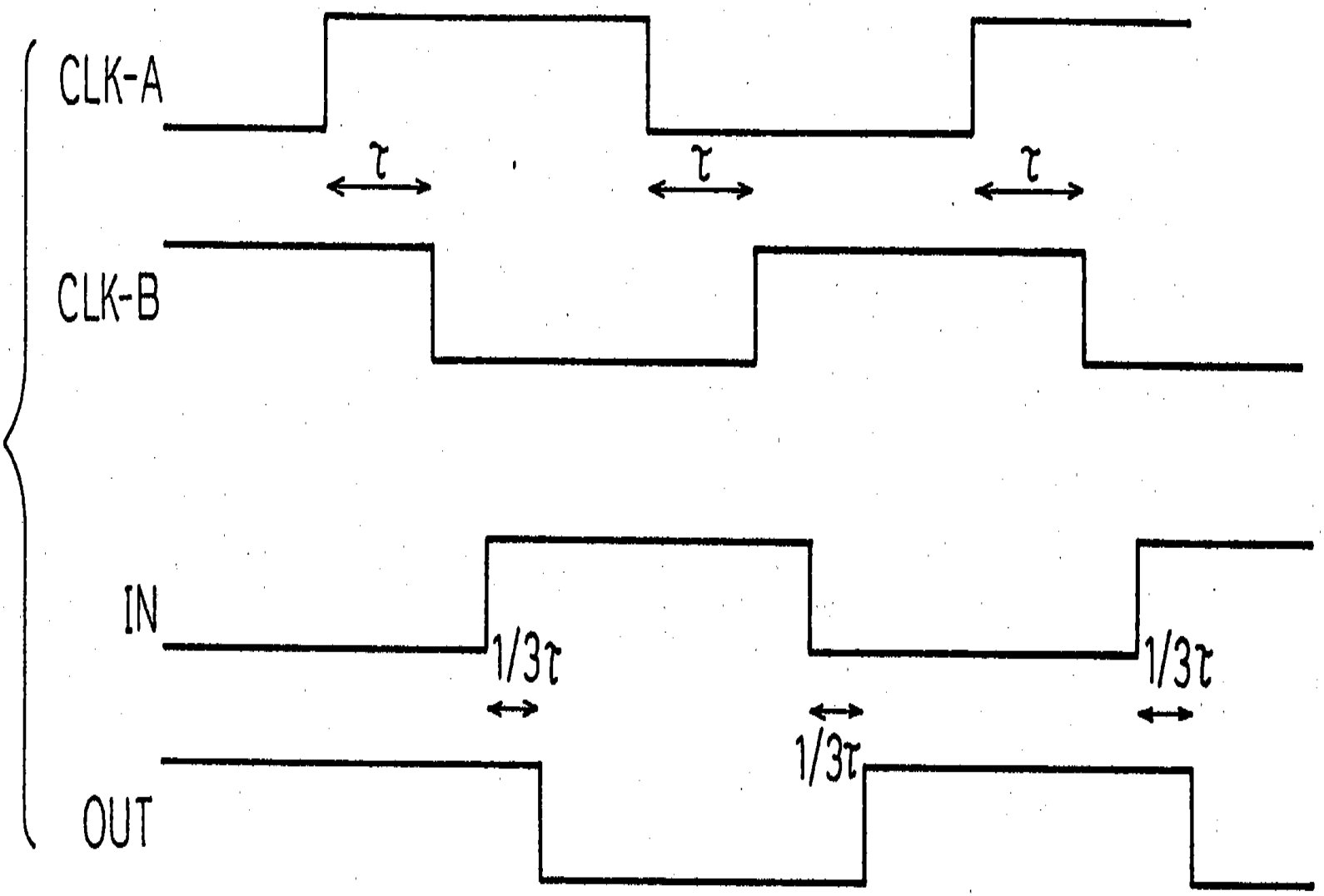


Fig.40A

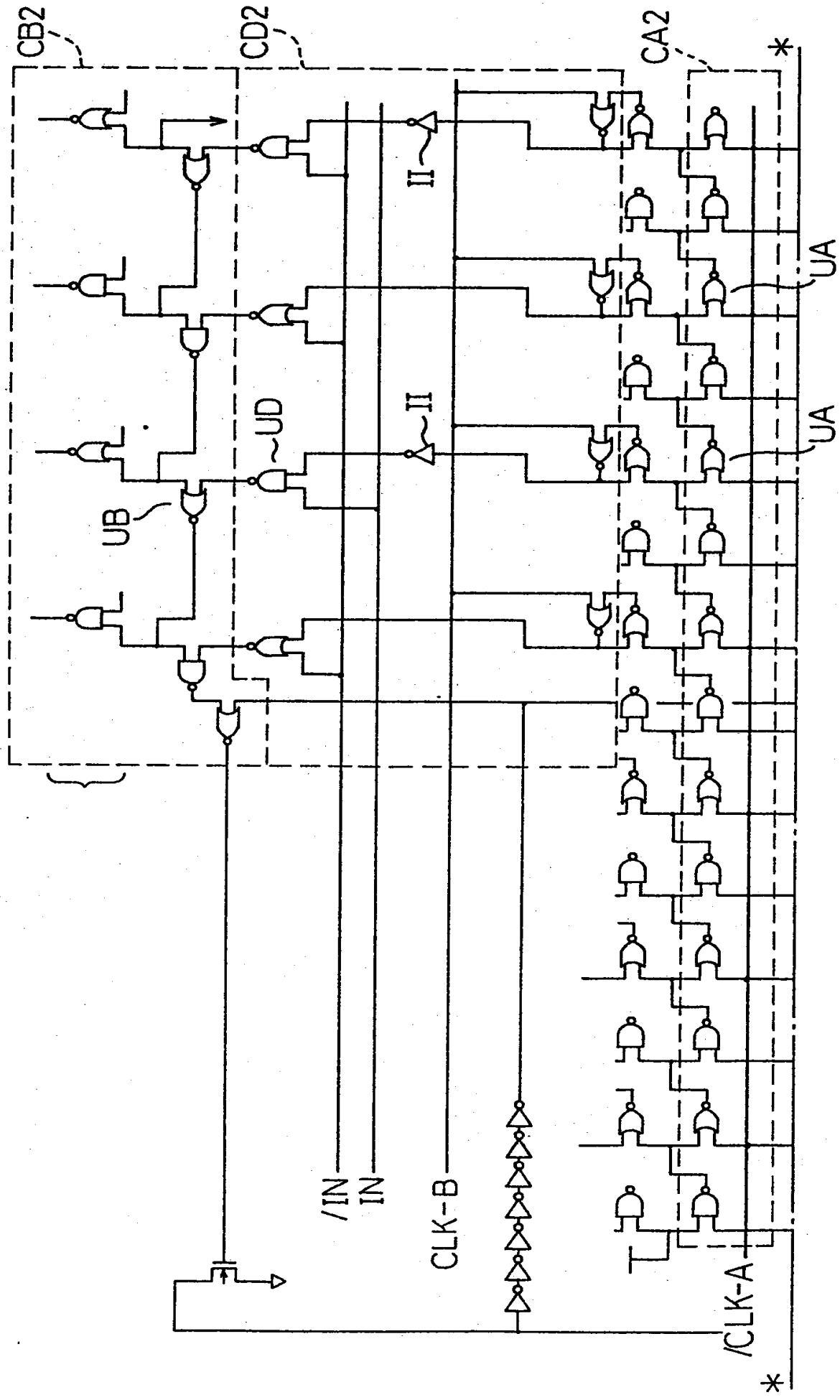


Fig. 40B

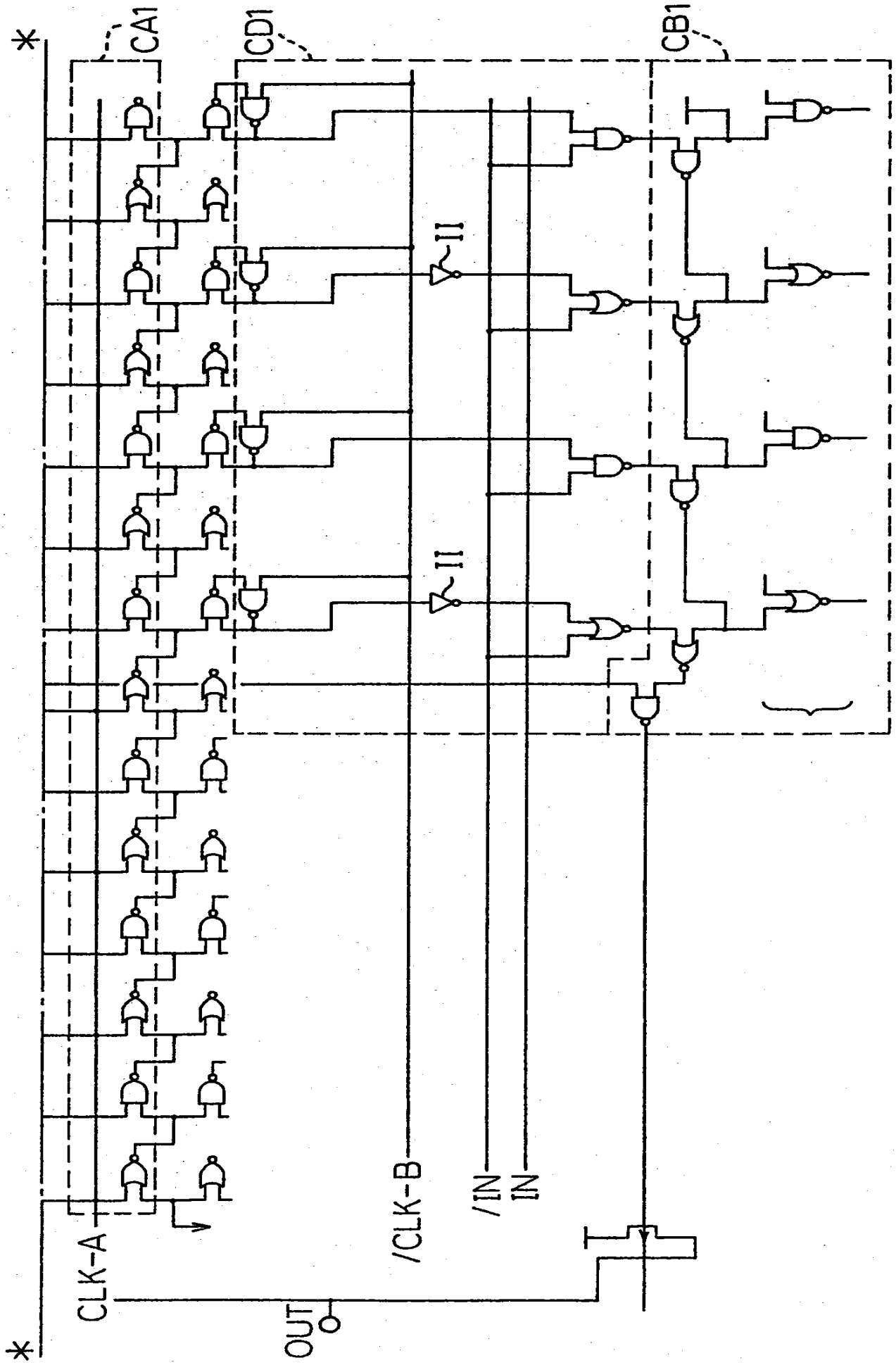


Fig.41

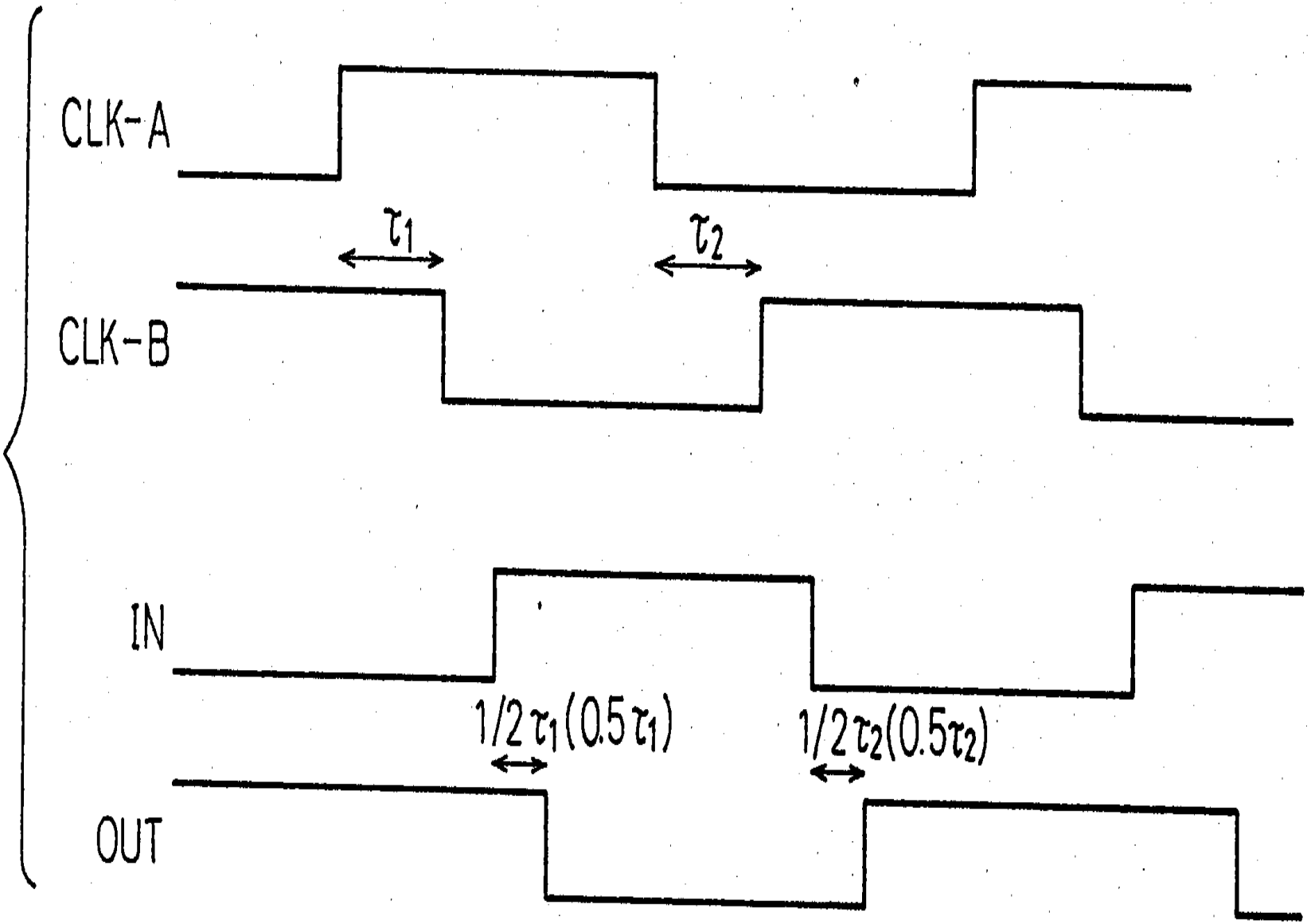


Fig. 42A

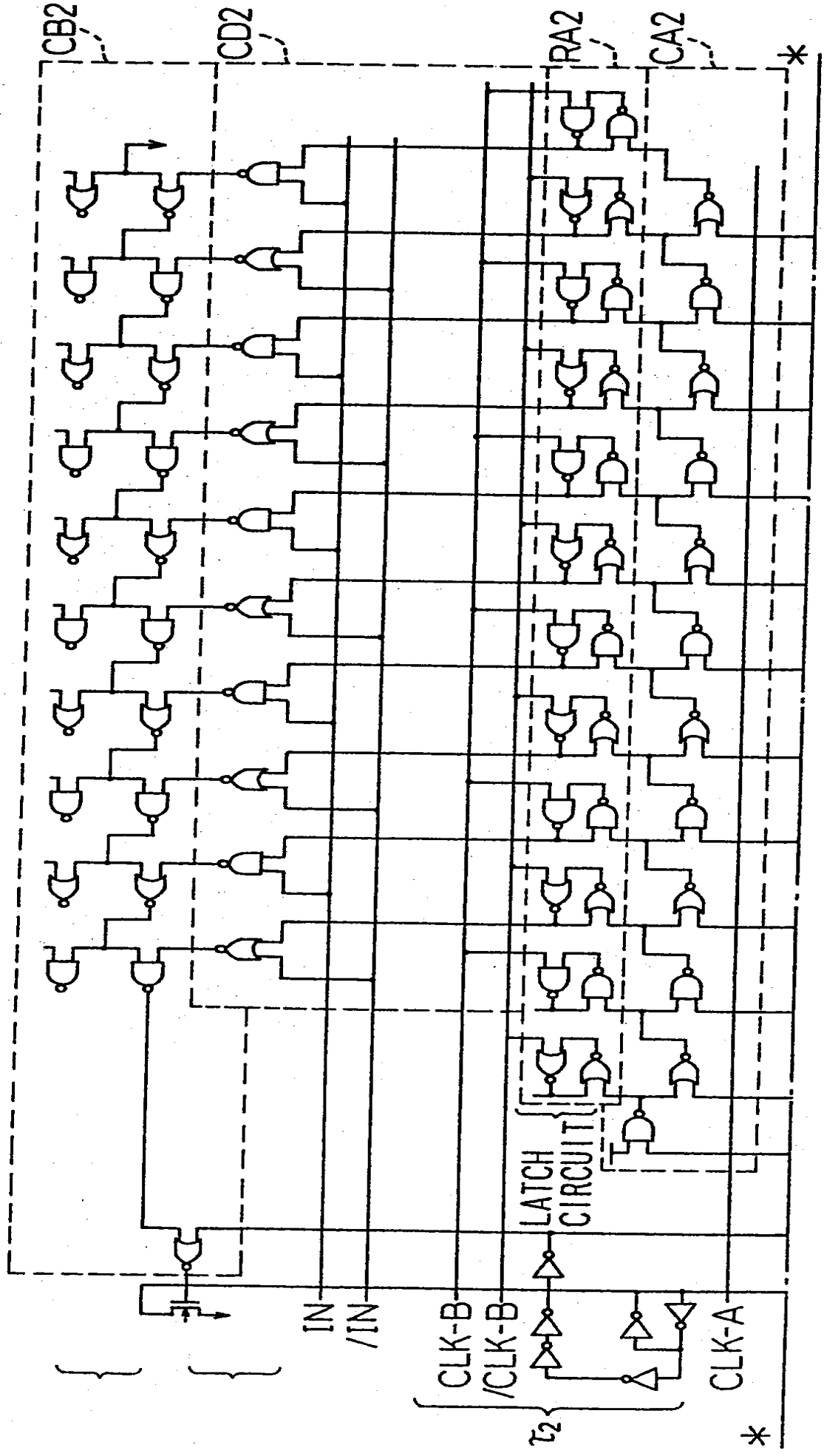


Fig. 42B

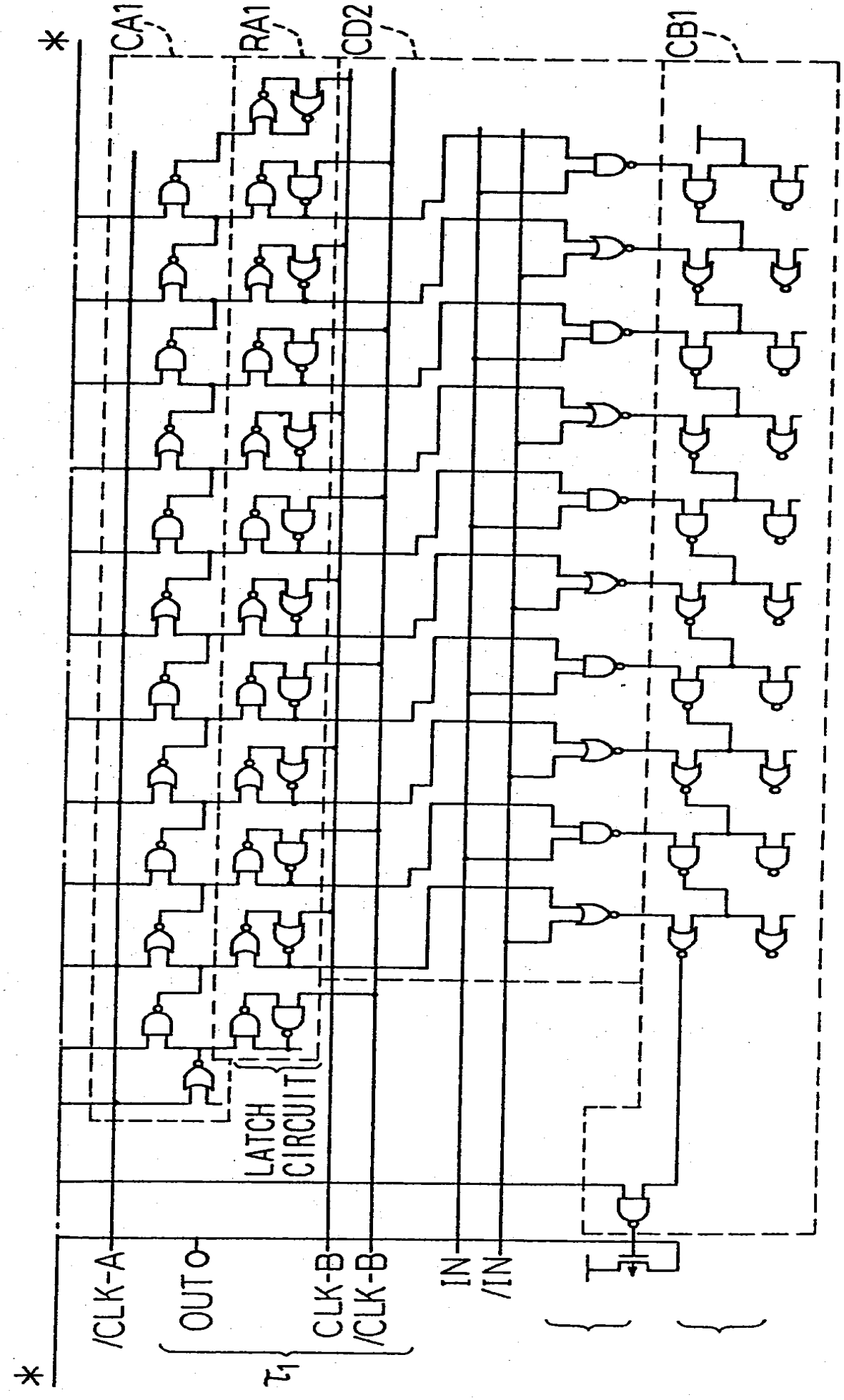


Fig. 43

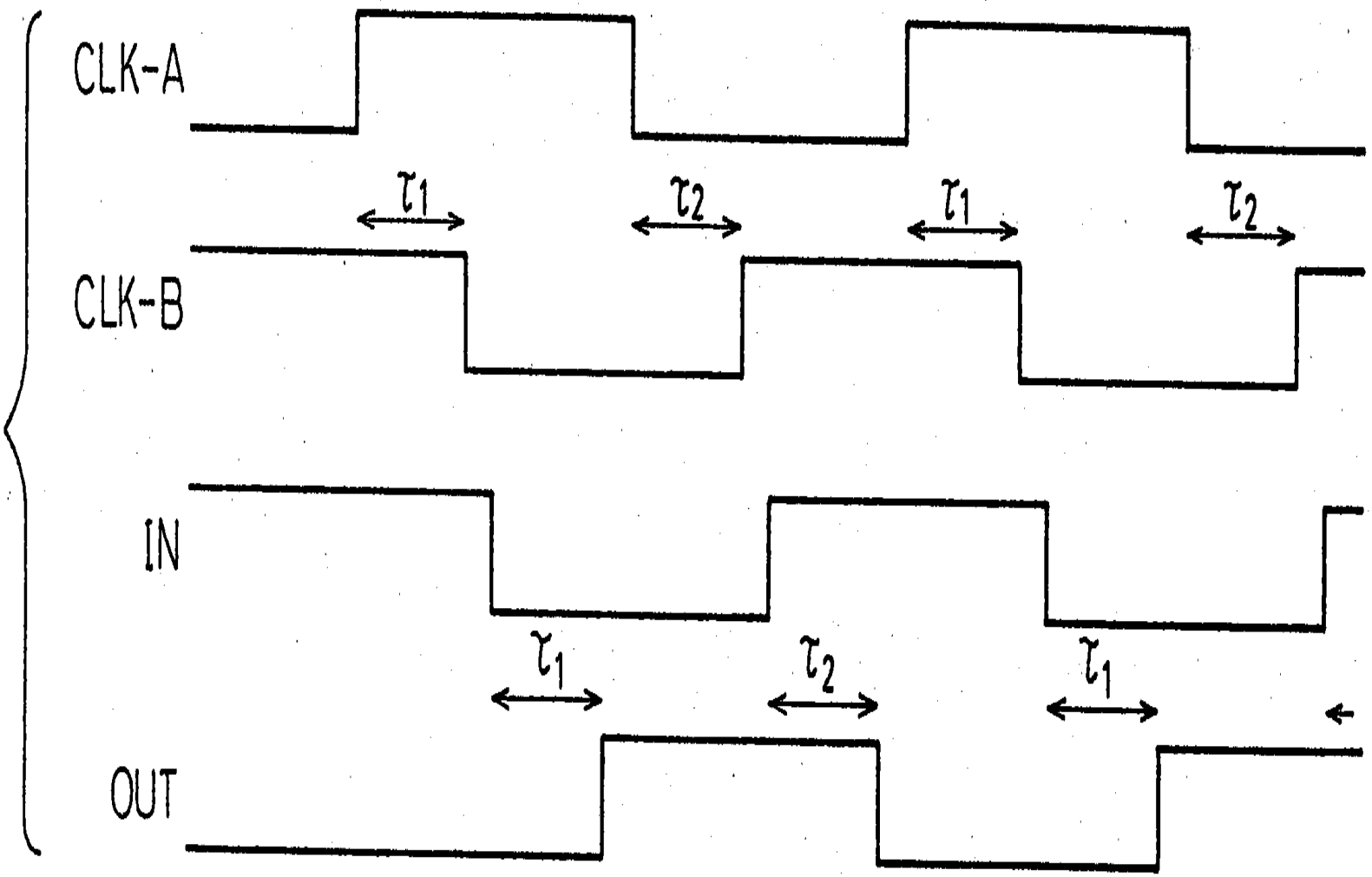


Fig.44A

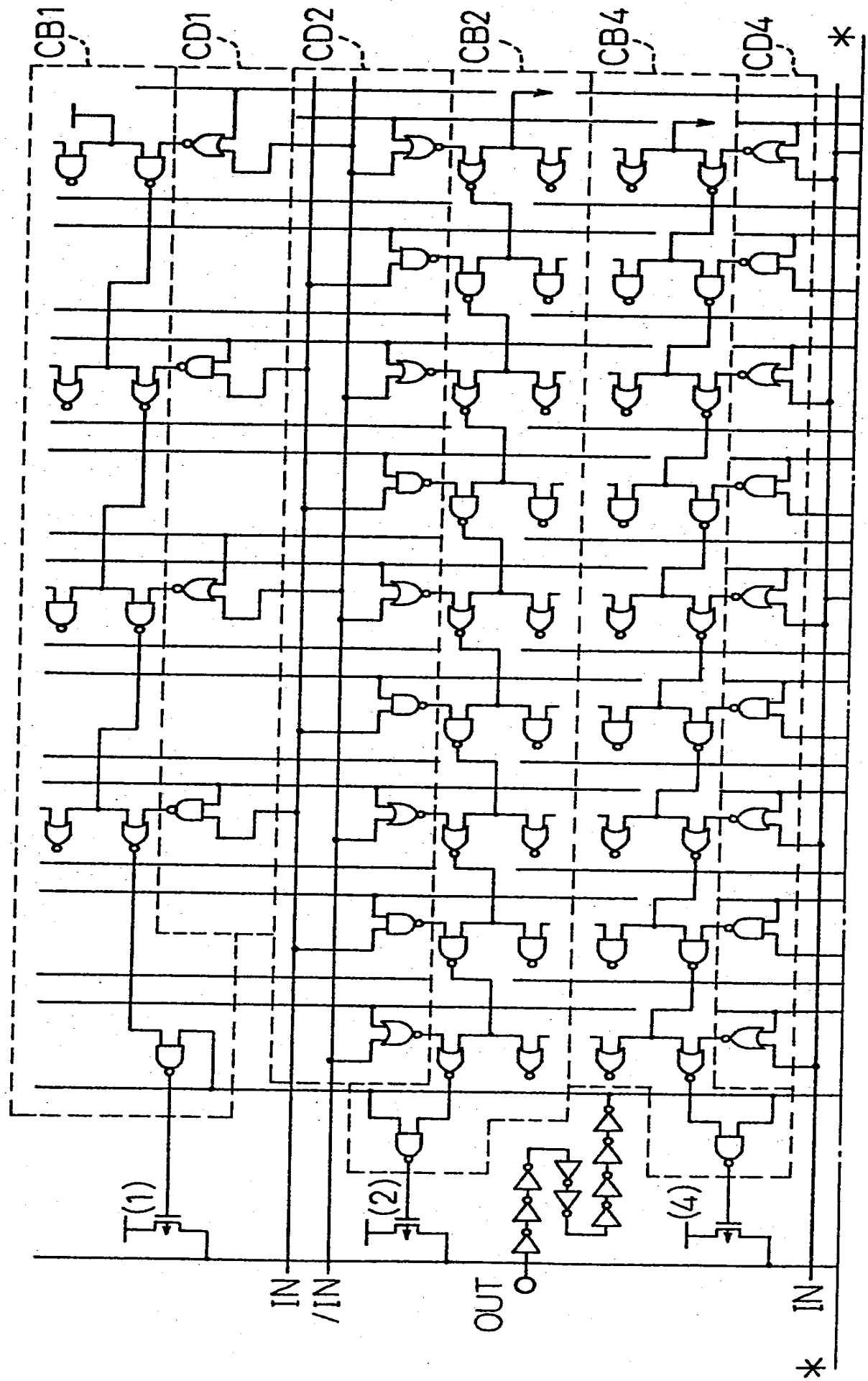


Fig. 44B

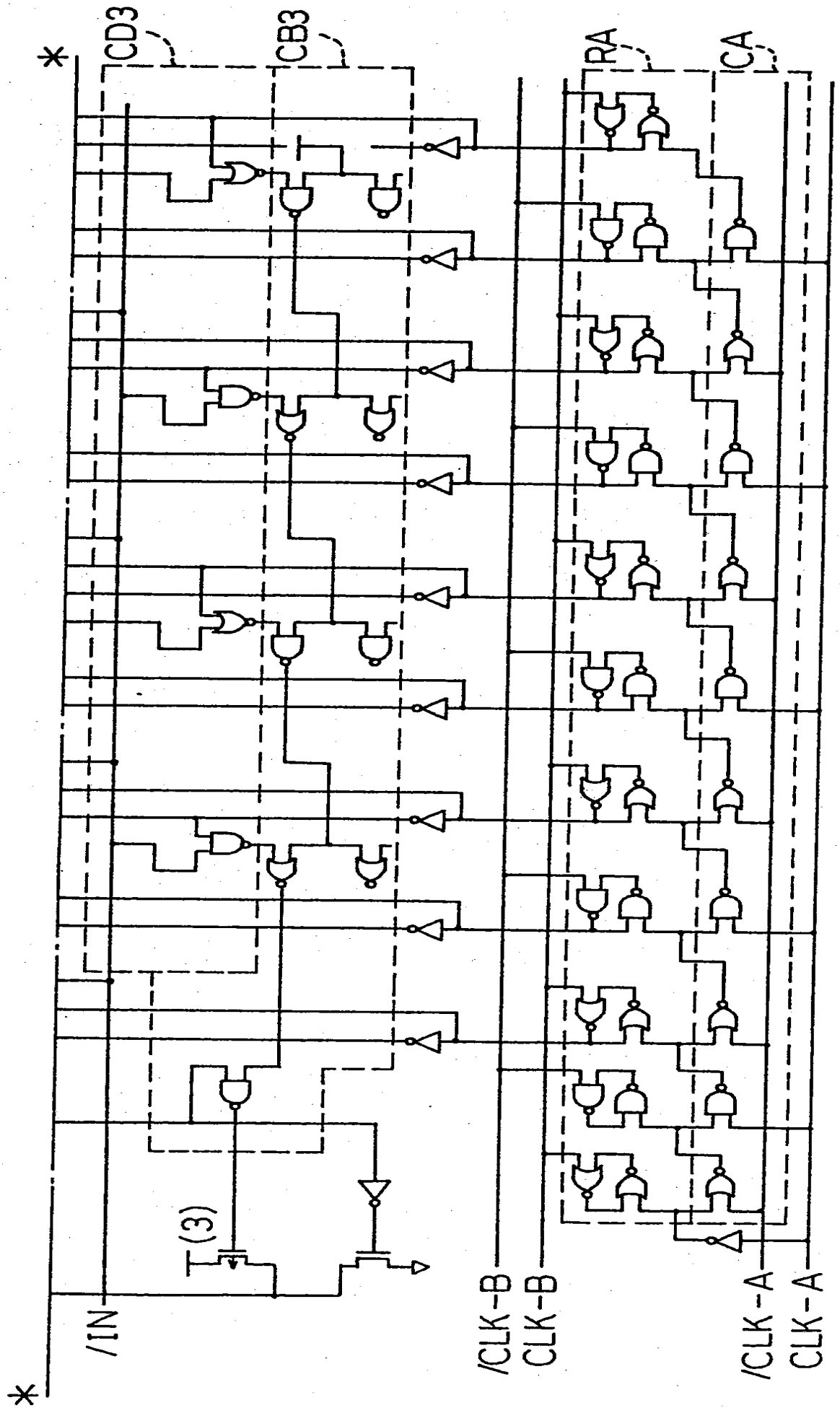


Fig.45

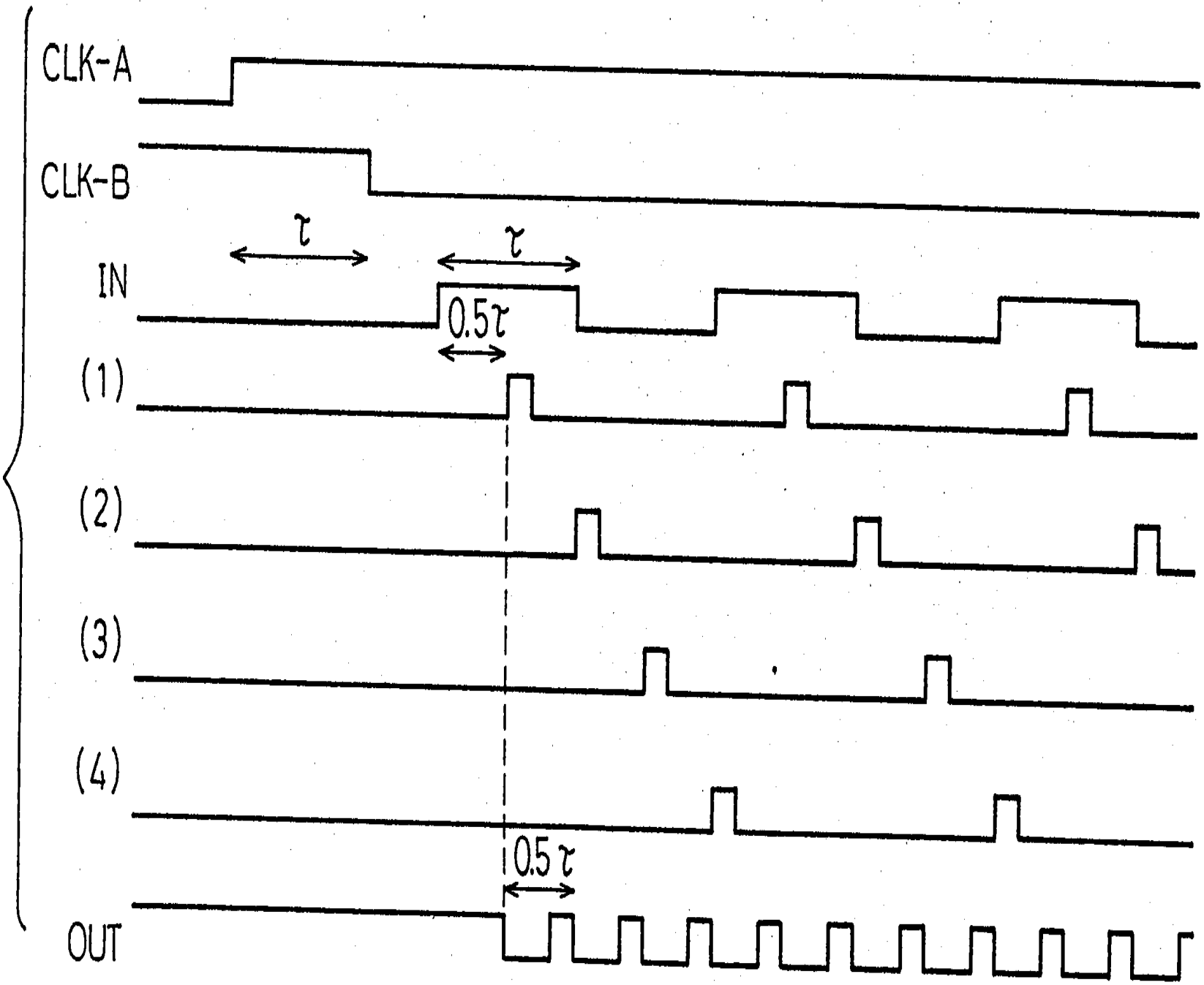


Fig.46

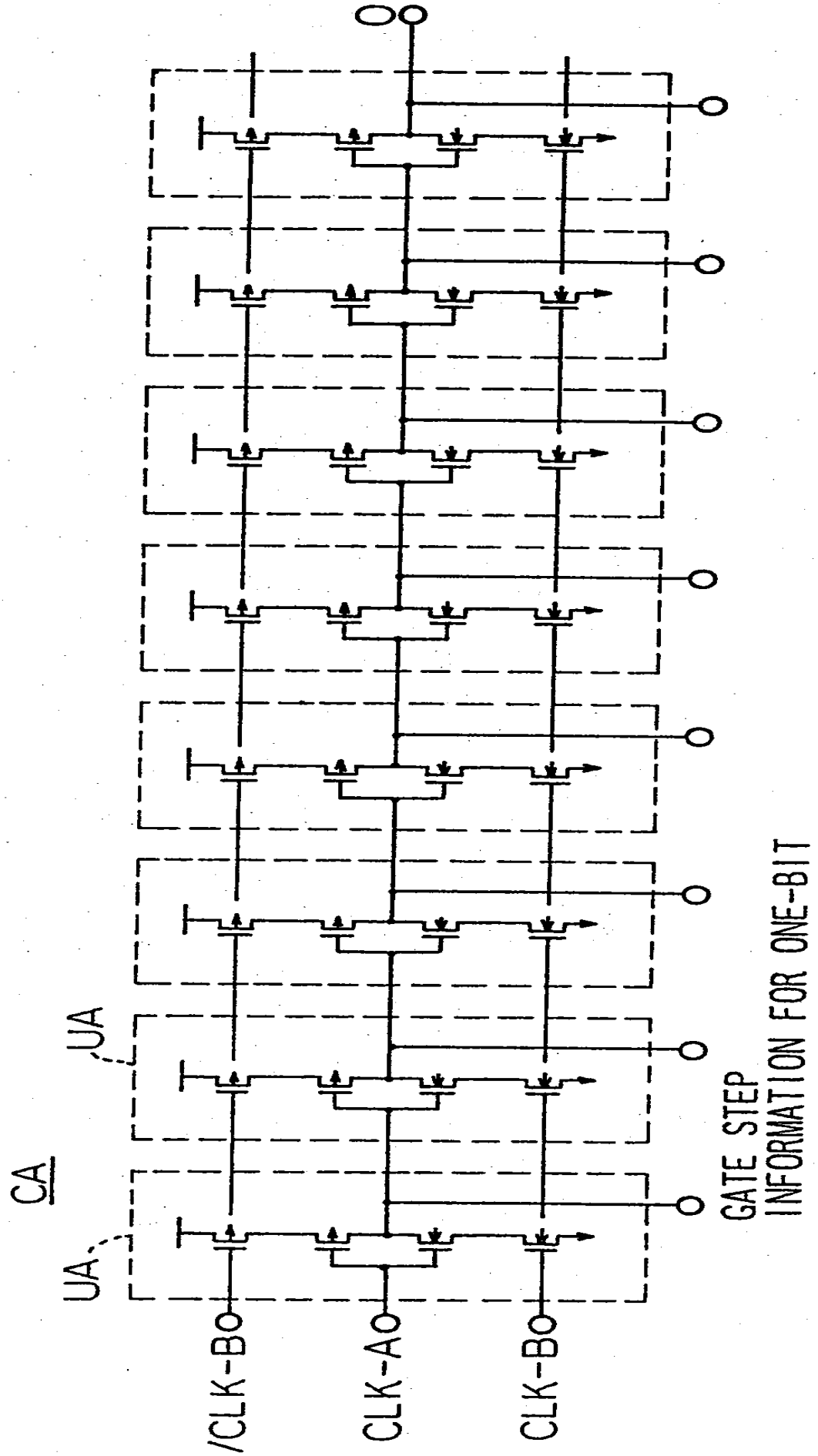


Fig. 47

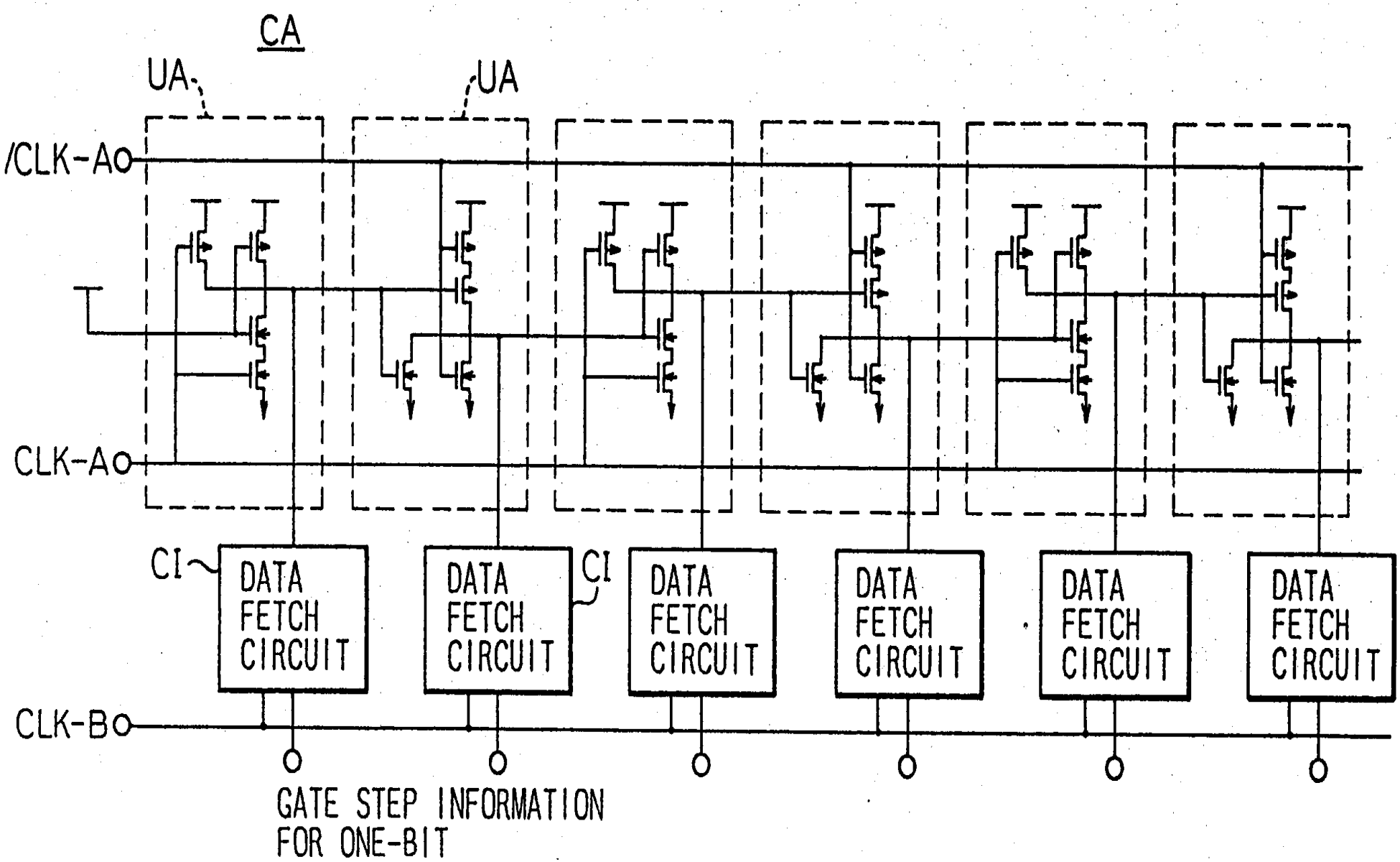

CA
UA
UA
/CLK-Ao
CLK-Ao
CI
DATA FETCH CIRCUIT
DATA FETCH CIRCUIT
CI
DATA FETCH CIRCUIT
DATA FETCH CIRCUIT
DATA FETCH CIRCUIT
DATA FETCH CIRCUIT
CLK-Bo
GATE STEP INFORMATION FOR ONE-BIT

Fig.48

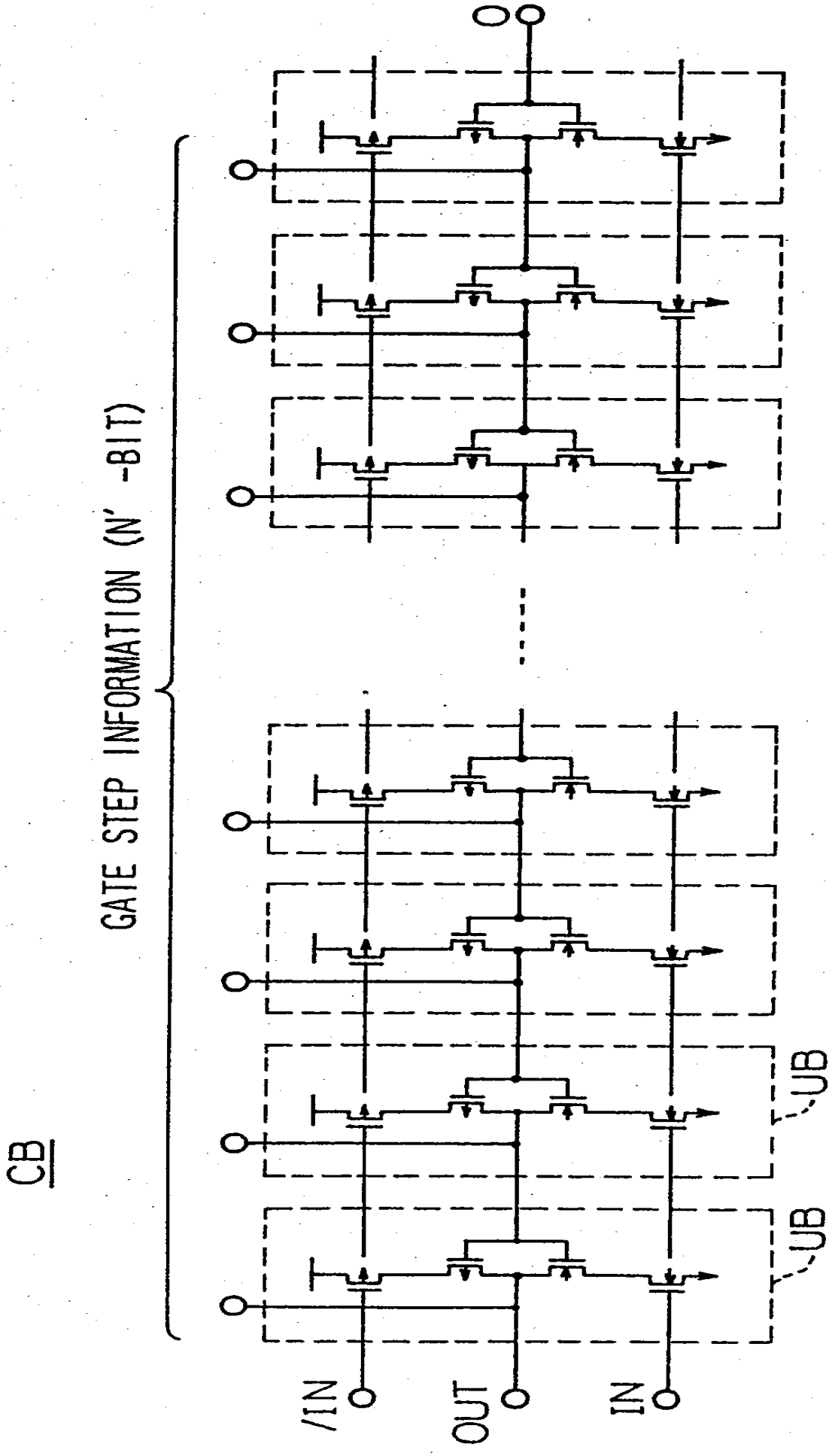


Fig. 49

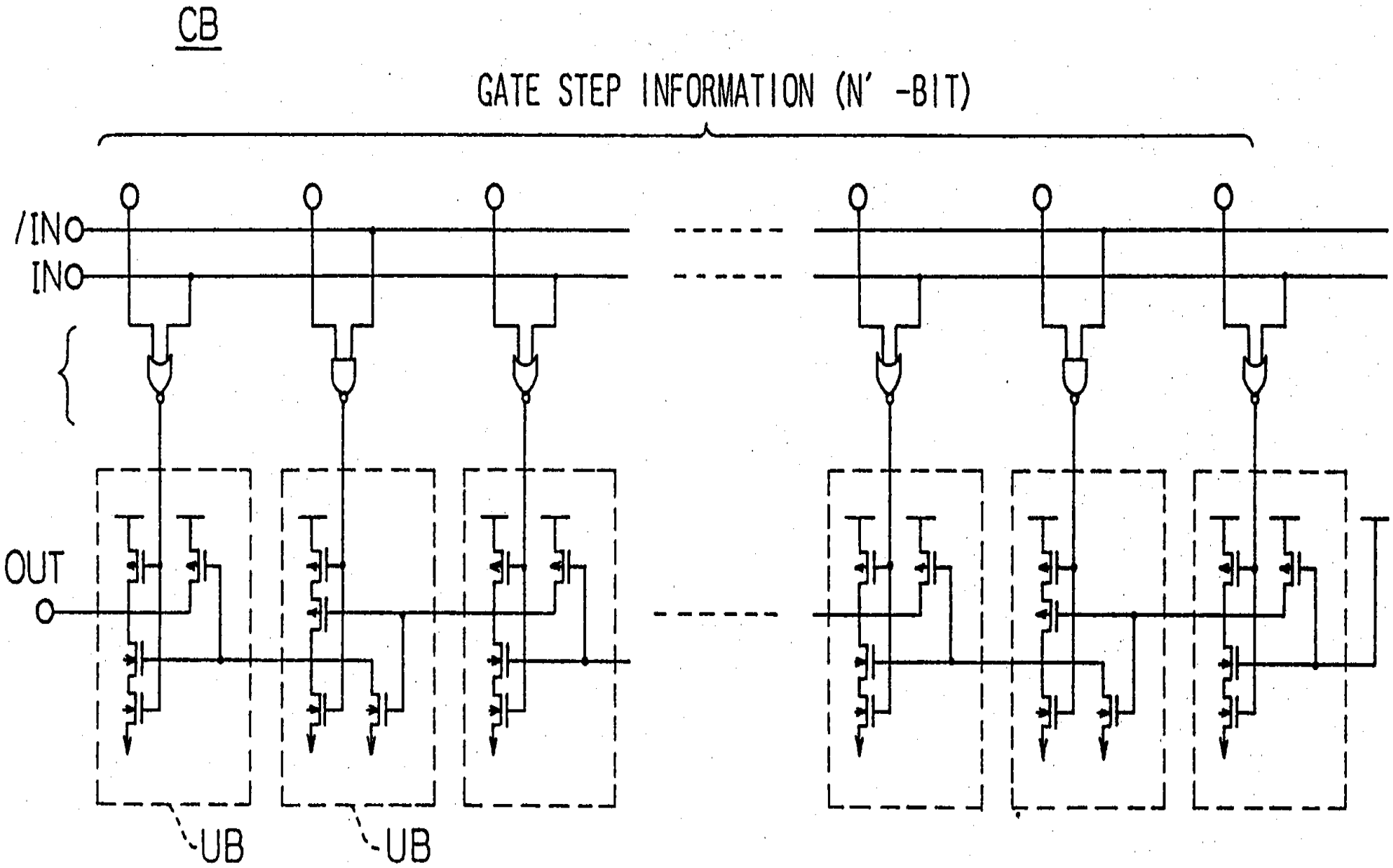


Fig.50A

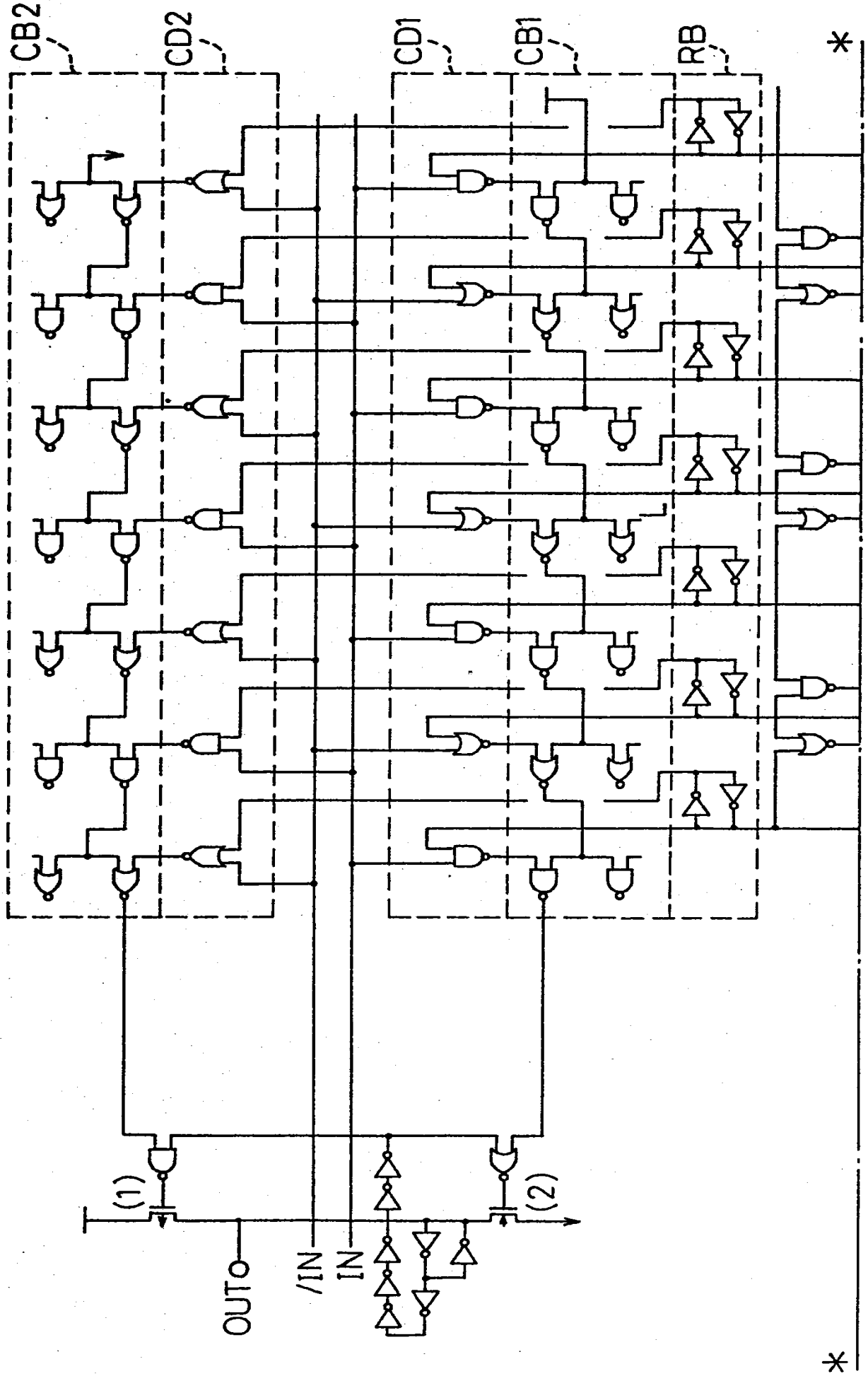


Fig.50B

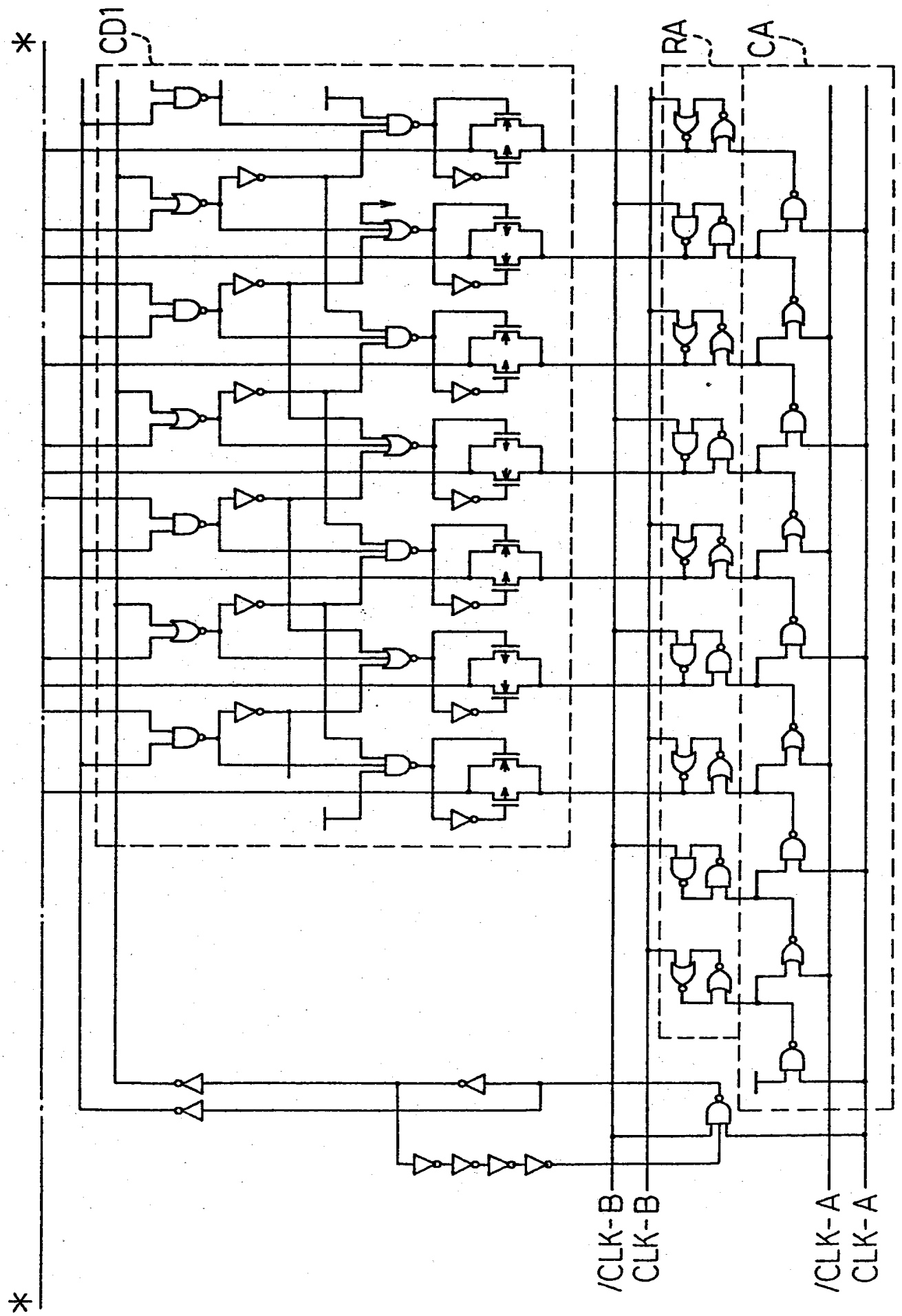


Fig. 51

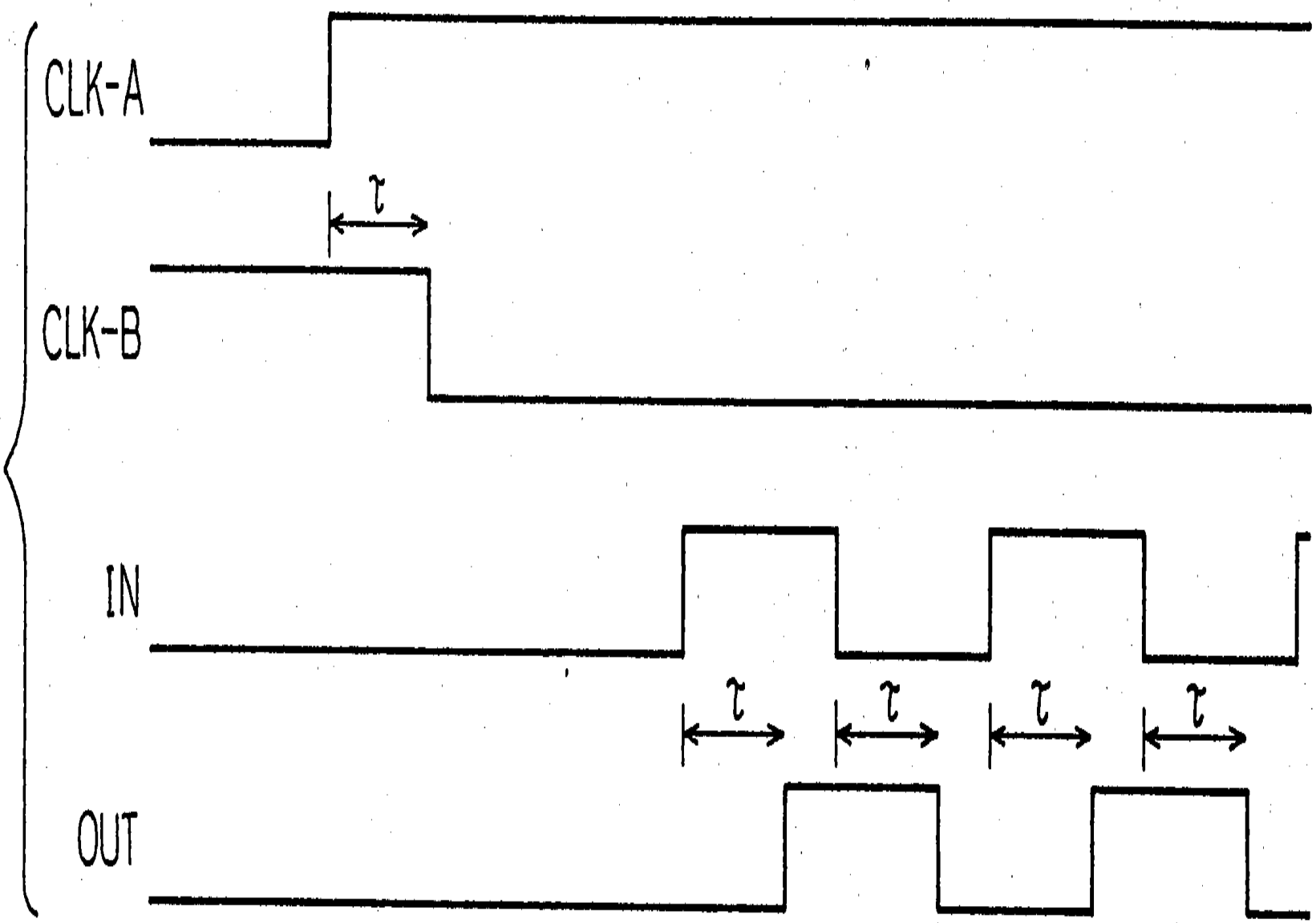


Fig. 52A

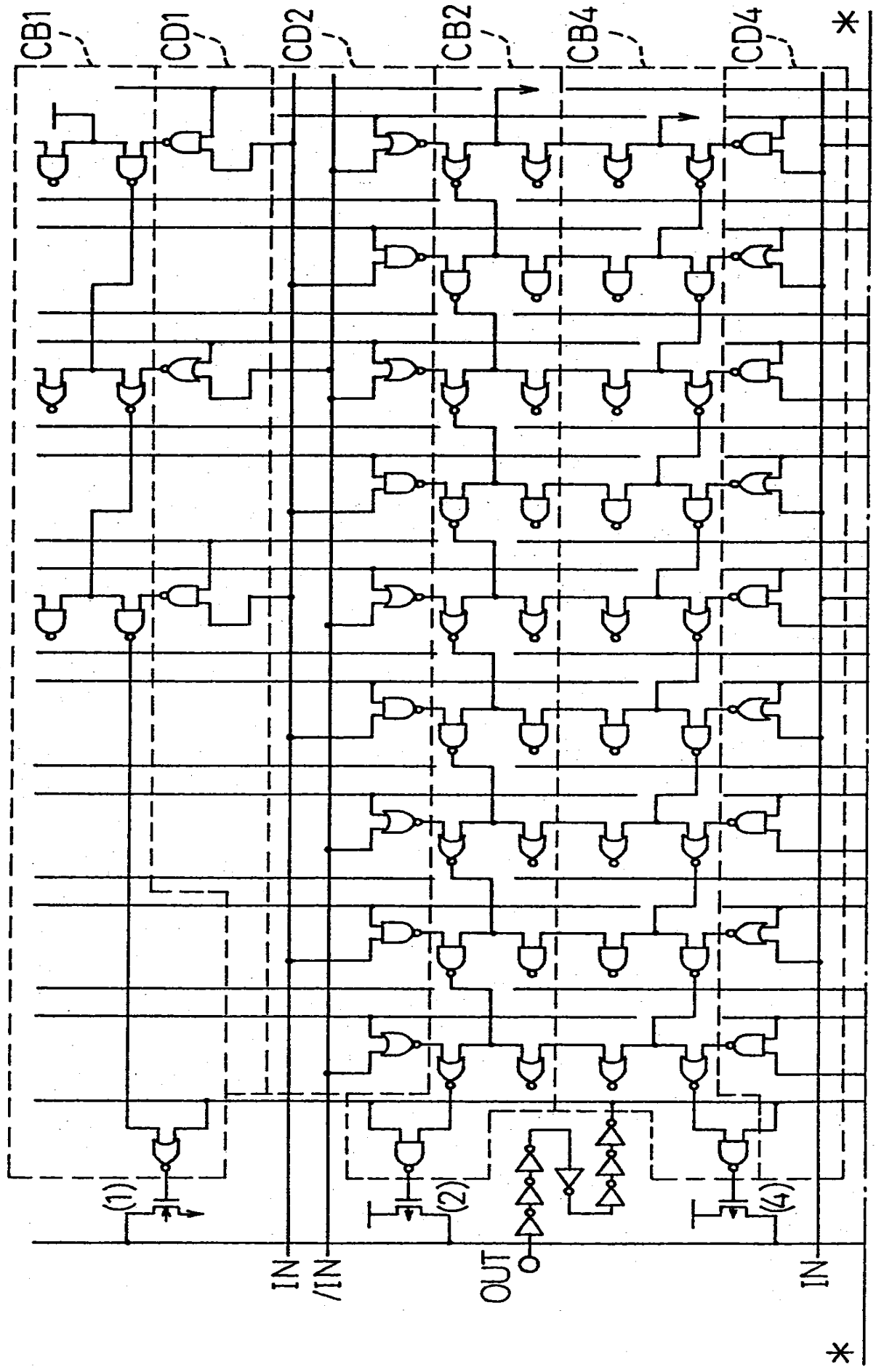


Fig. 52B

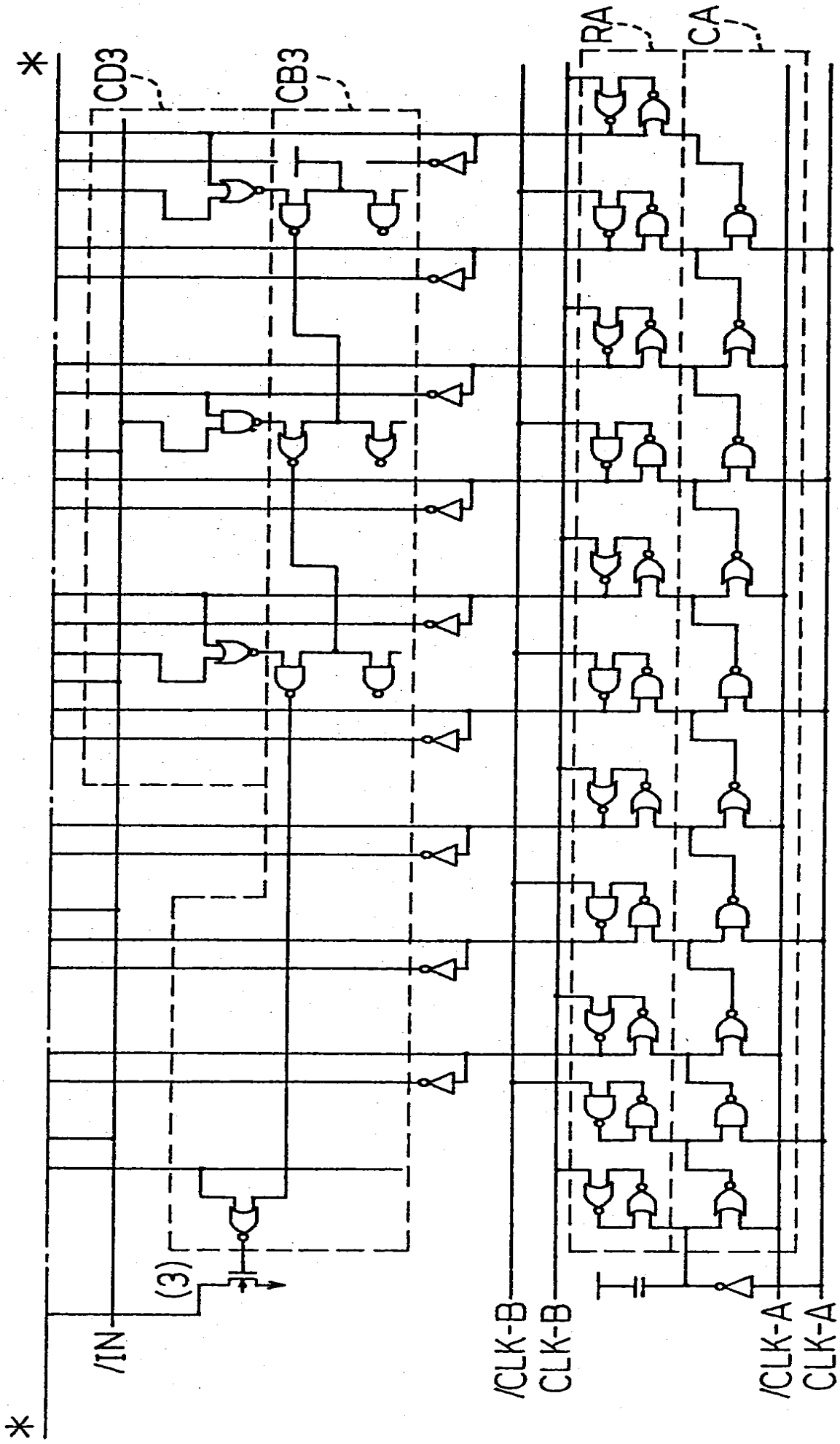


Fig. 53

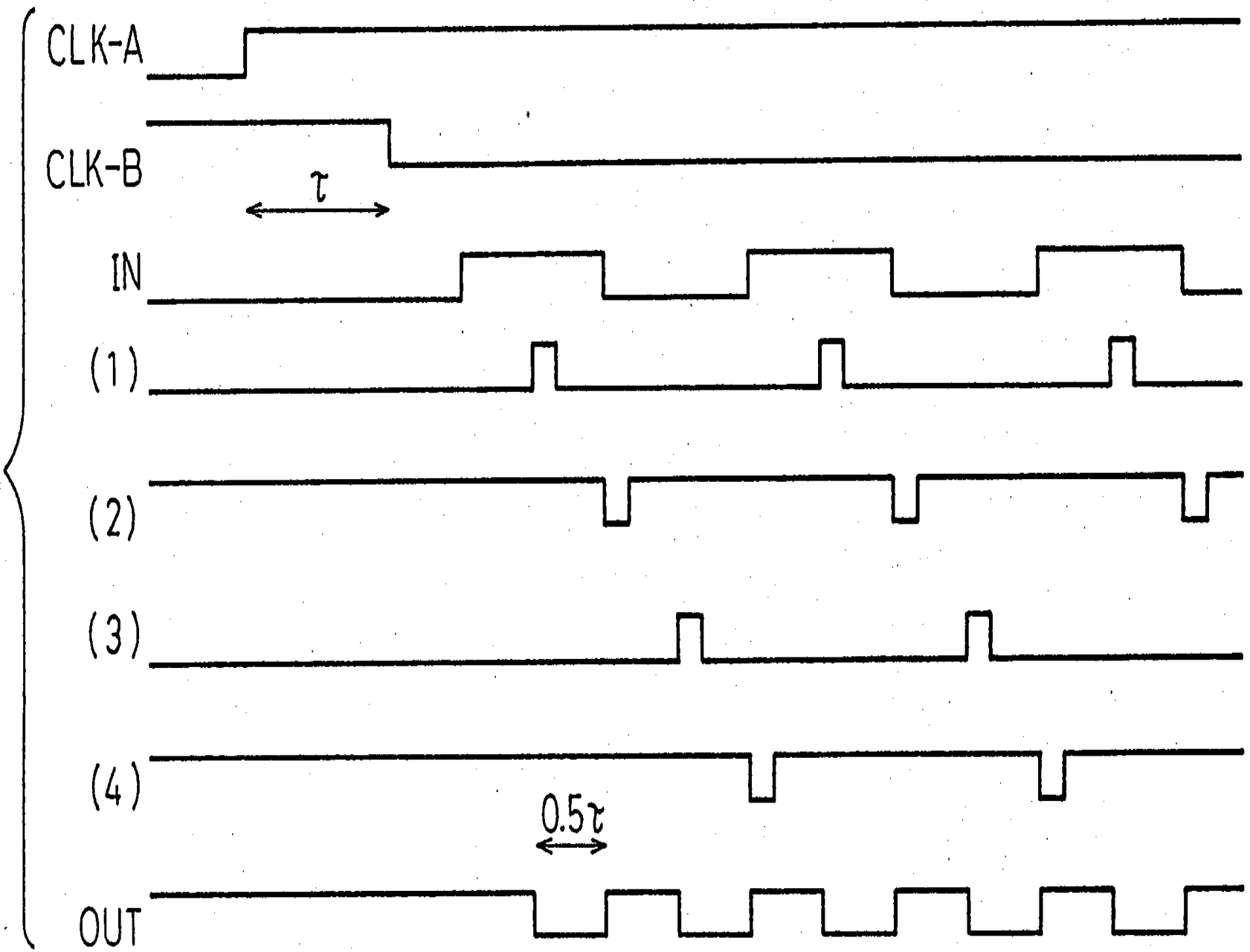


Fig. 54A

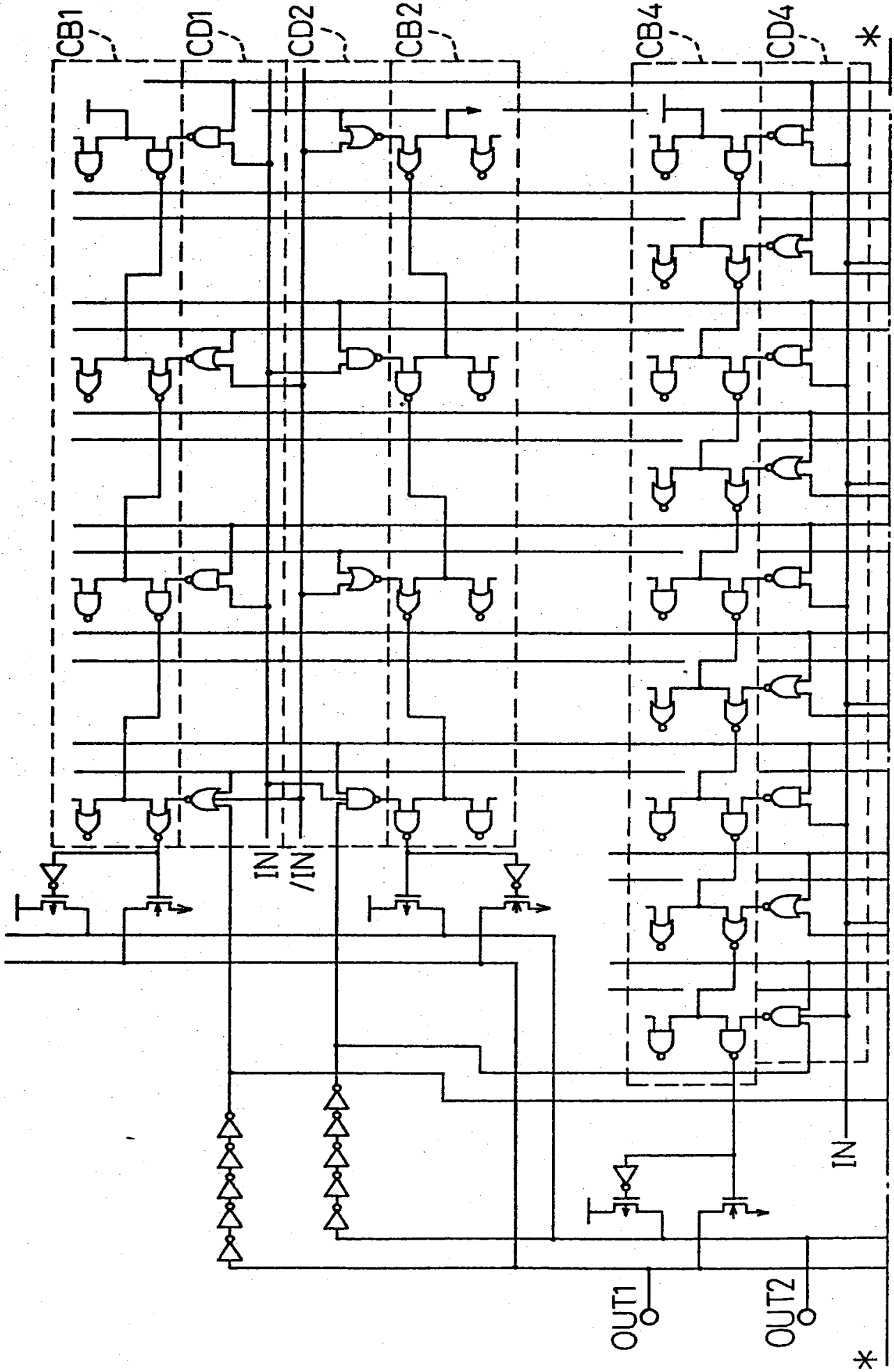


Fig. 54B

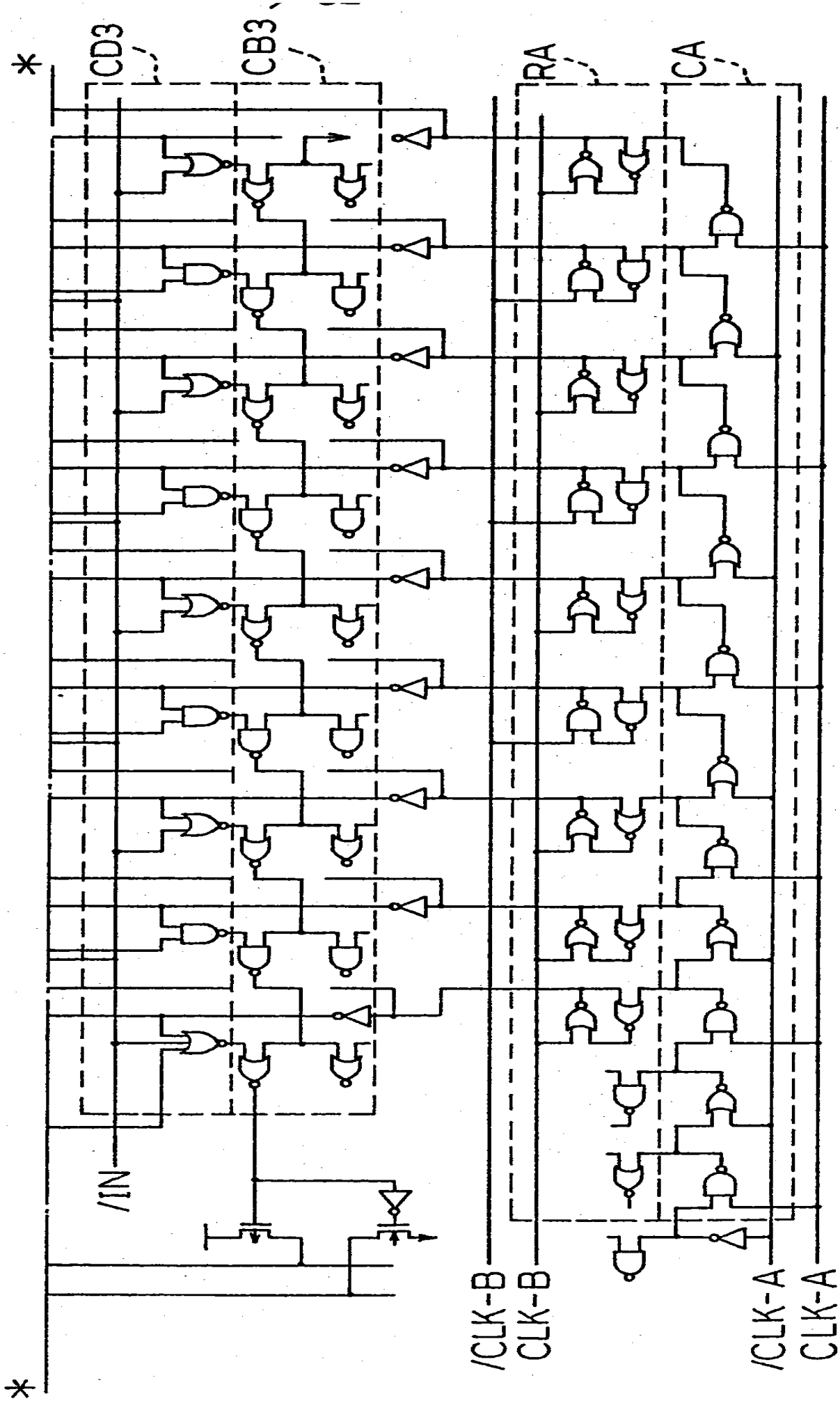


Fig.55

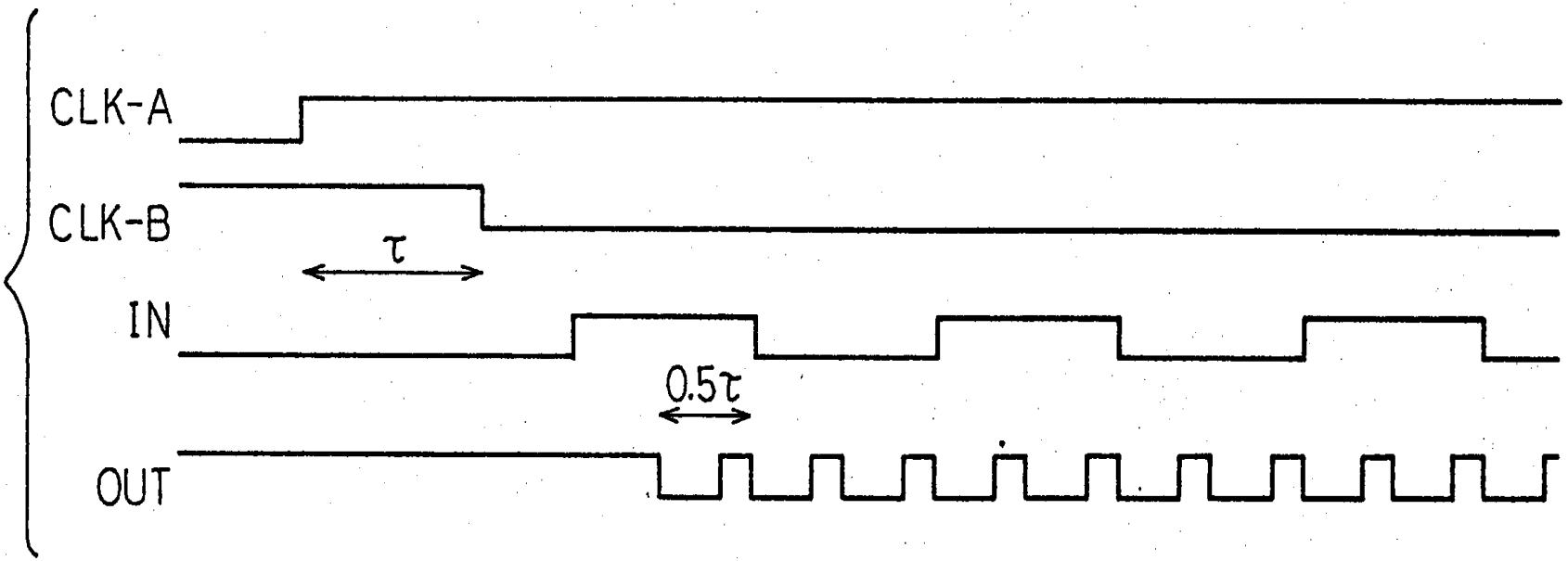


Fig. 56A

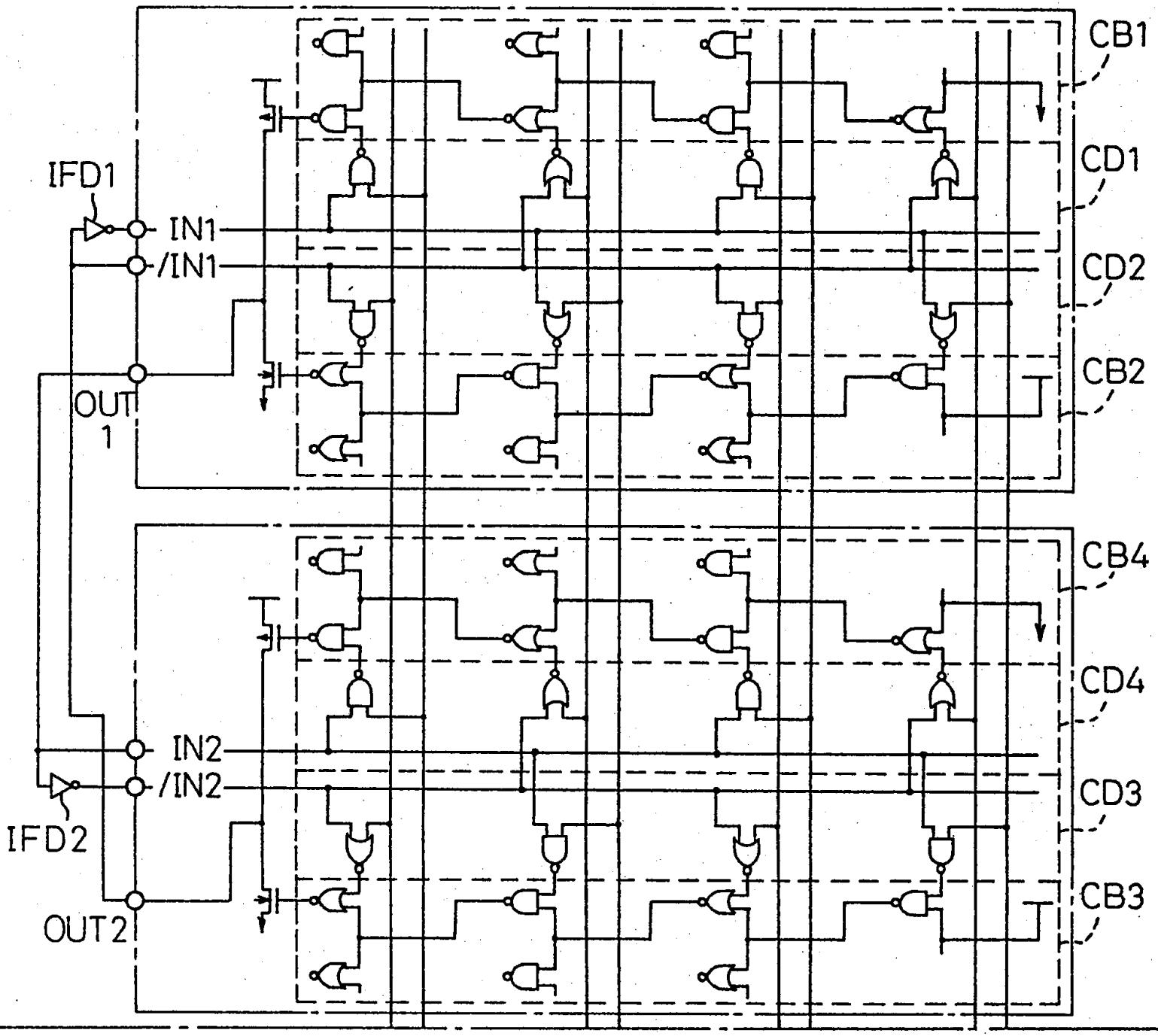

CB1
CD1
CD2
CB2
IFD1
IN1
/IN1
OUT 1
CB4
CD4
IN2
/IN2
CD3
IFD2
CB3
OUT2
*
*

Fig. 56B

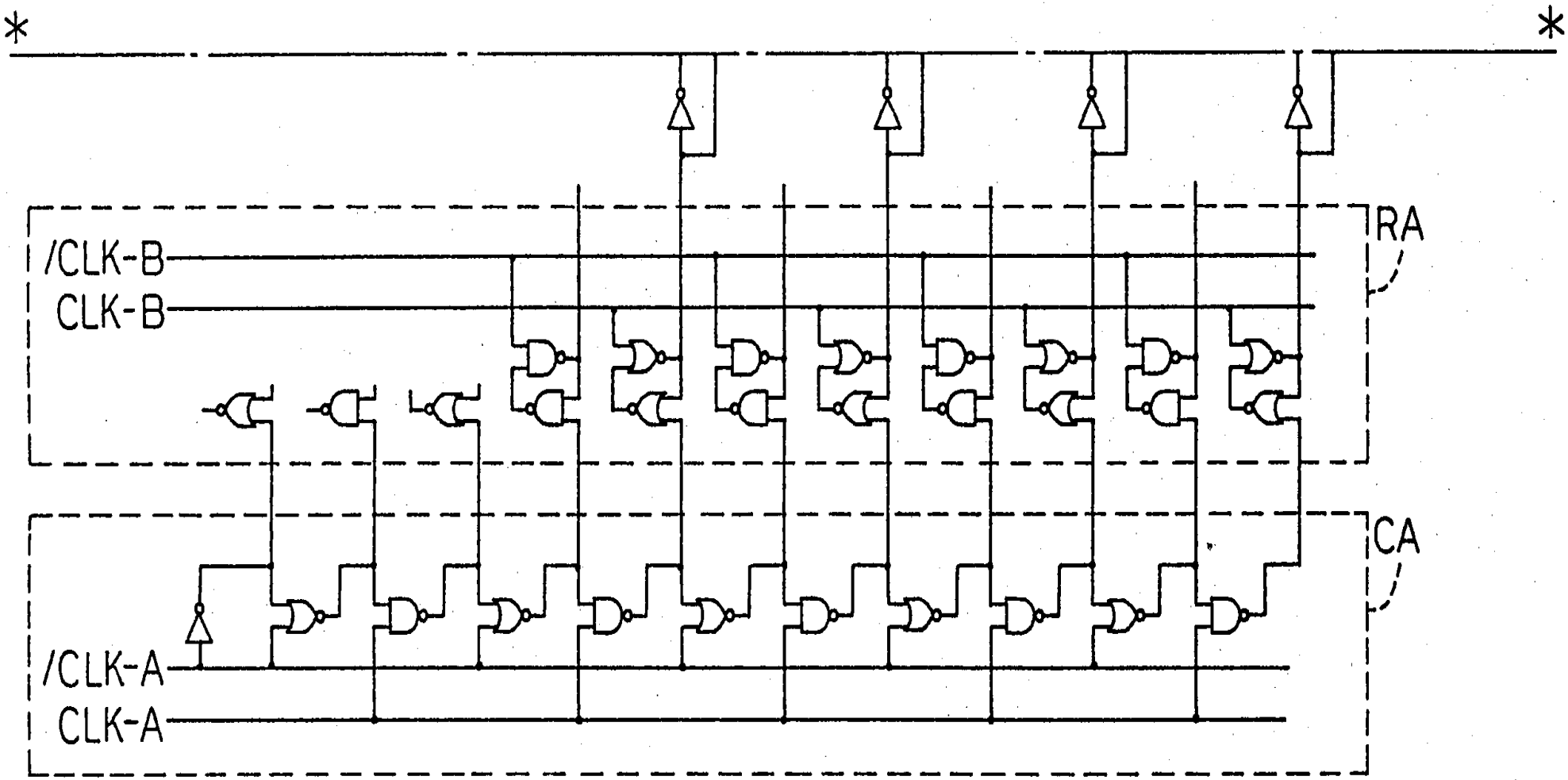


Fig. 57

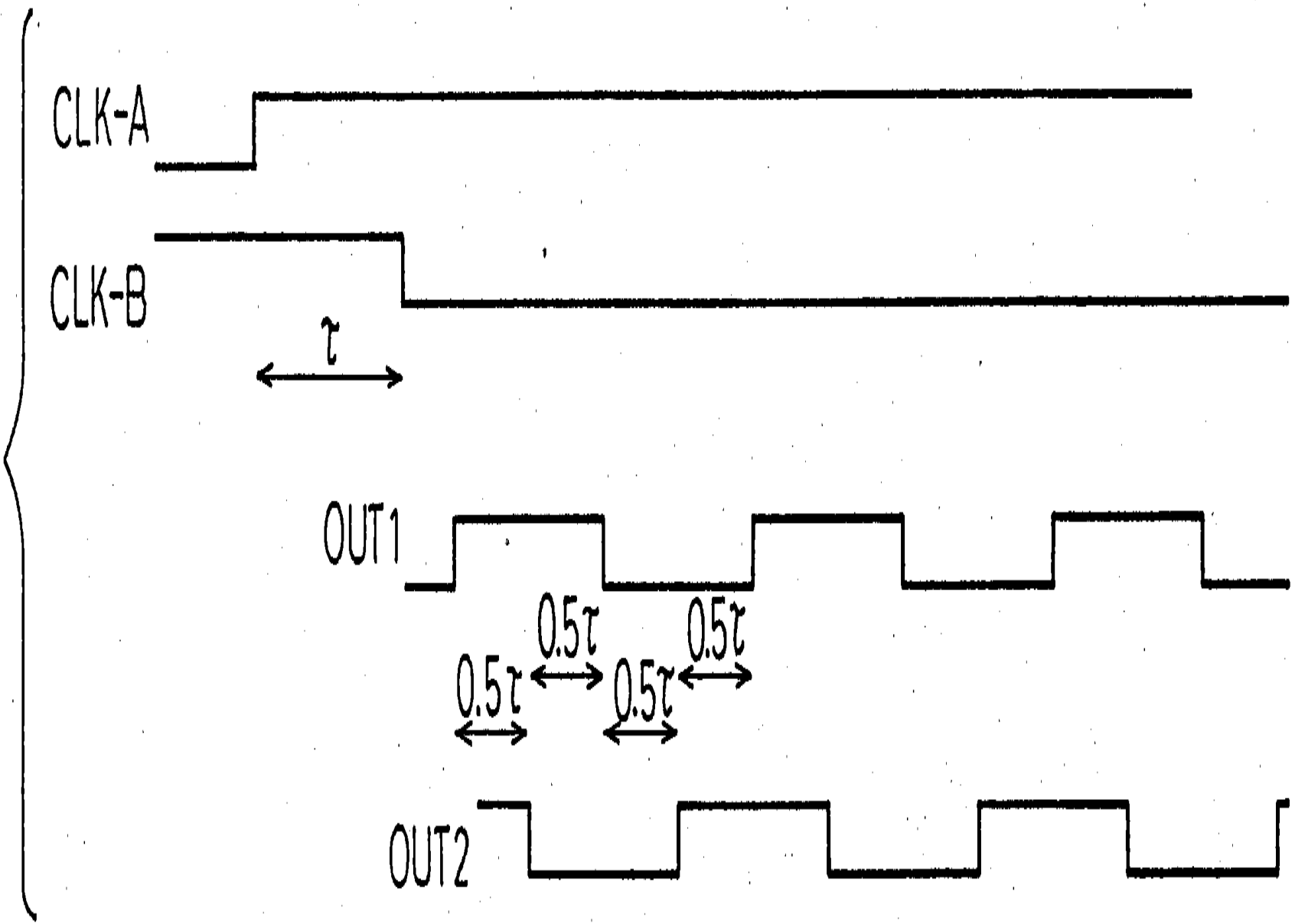


Fig.58A

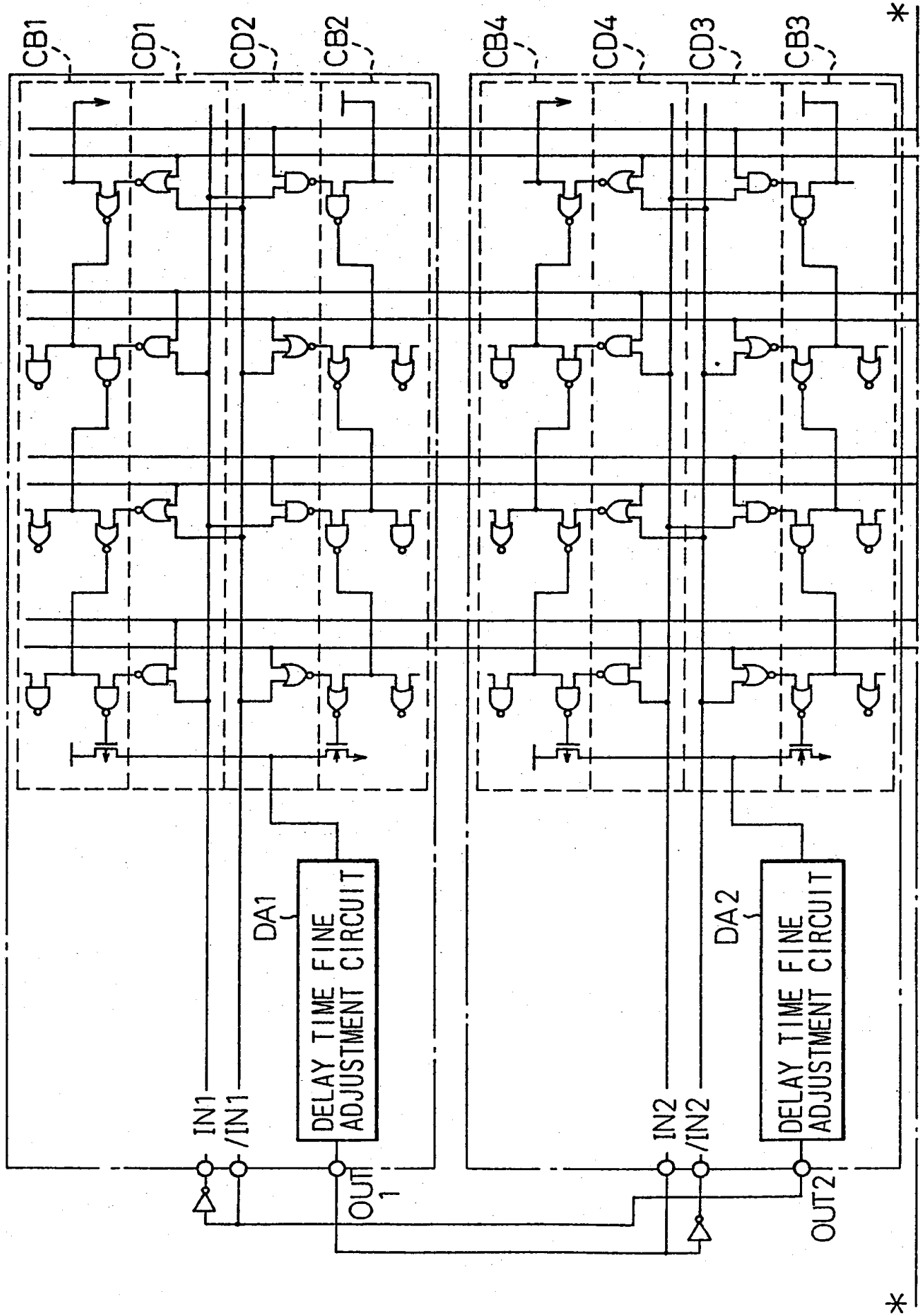

CB1
CD1
CD2
CB2
CB4
CD4
CD3
CB3
DA1
DELAY TIME FINE ADJUSTMENT CIRCUIT
DA2
DELAY TIME FINE ADJUSTMENT CIRCUIT
IN1
/IN1
IN2
/IN2
OUT1
OUT2

Fig. 58B

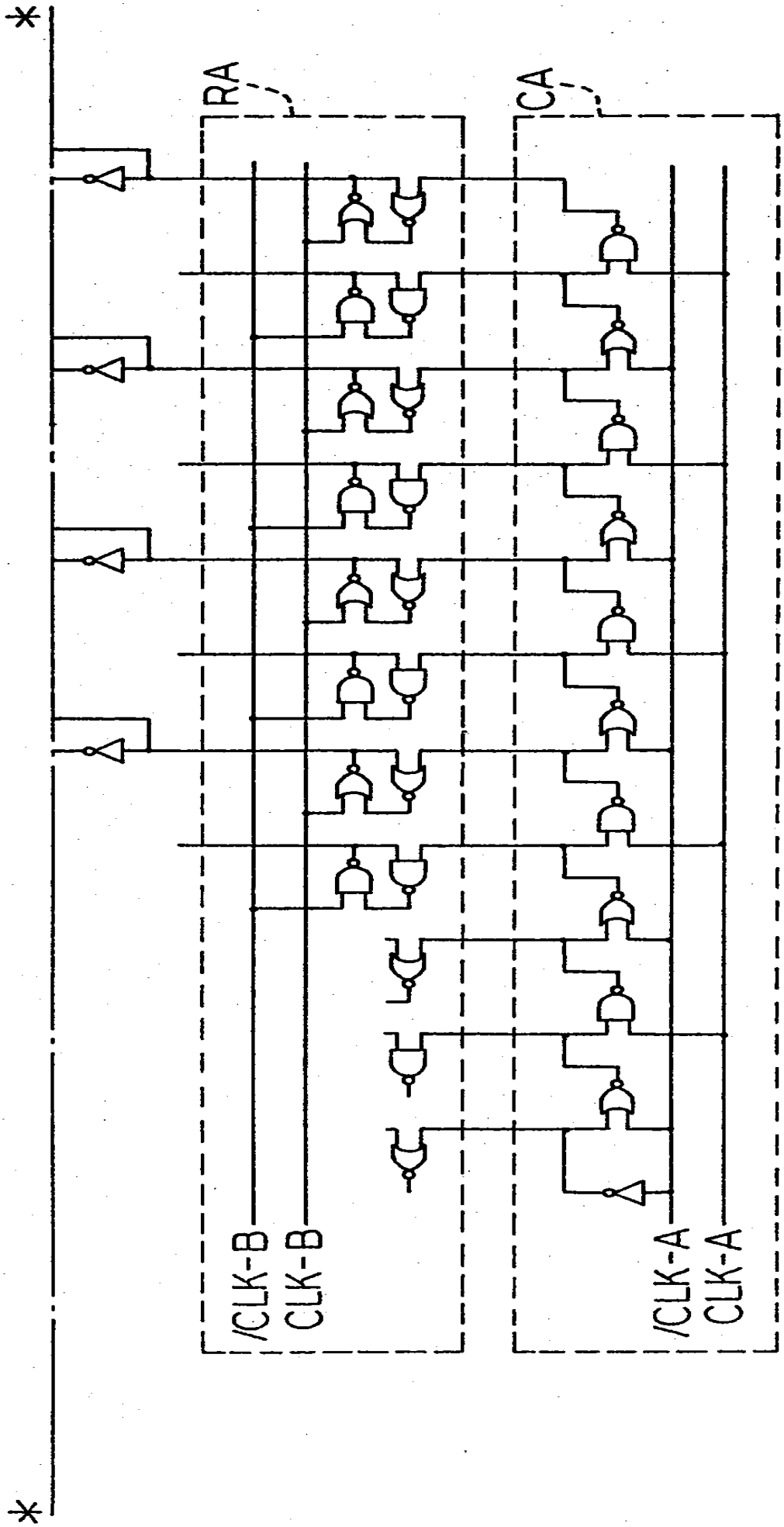


Fig.59

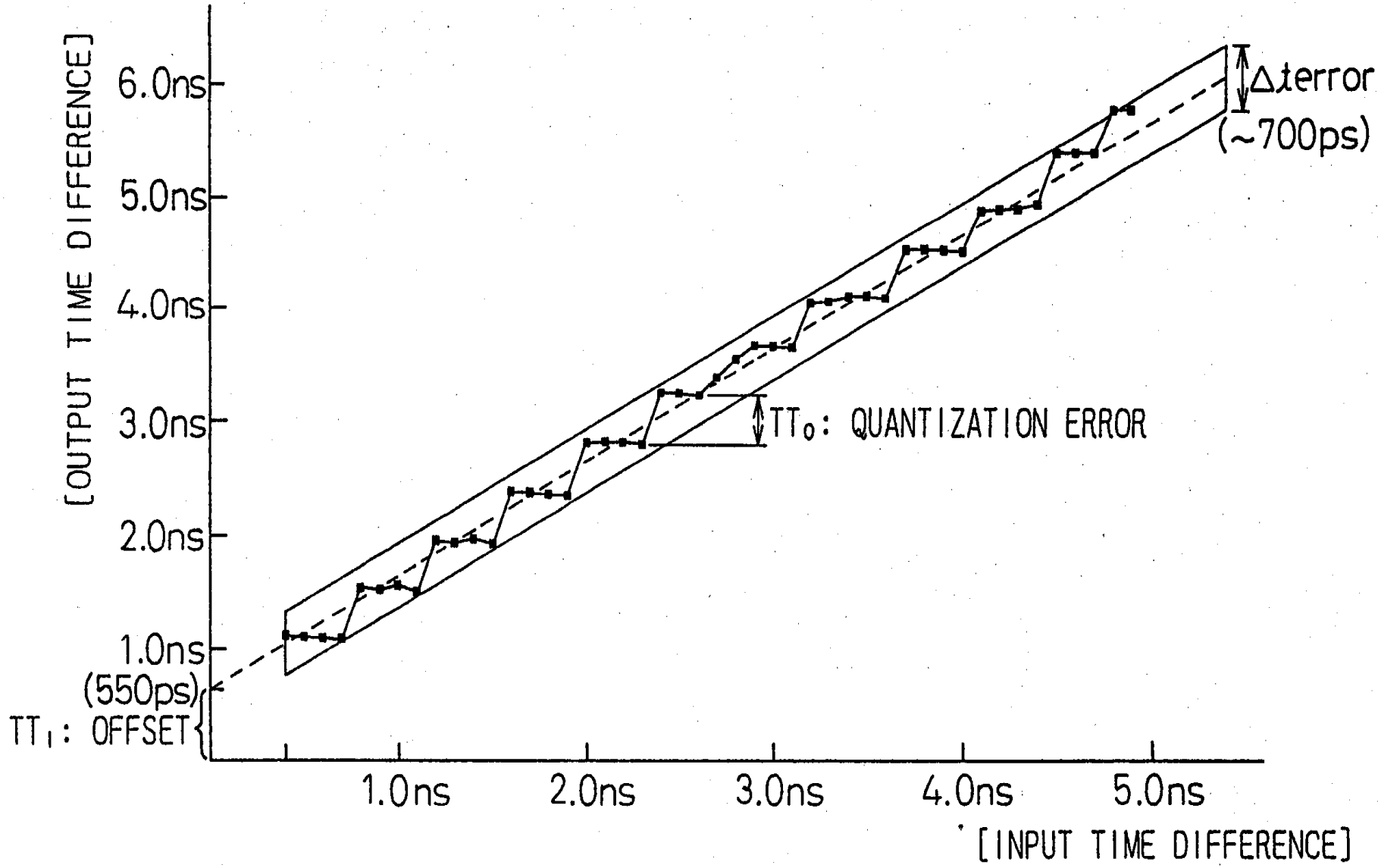

[OUTPUT TIME DIFFERENCE]
6.0ns
5.0ns
4.0ns
3.0ns
2.0ns
1.0ns
(550ps)
TT1: OFFSET
Δterror
(~700ps)
TT0: QUANTIZATION ERROR
1.0ns
2.0ns
3.0ns
4.0ns
5.0ns
[INPUT TIME DIFFERENCE]

Fig.60

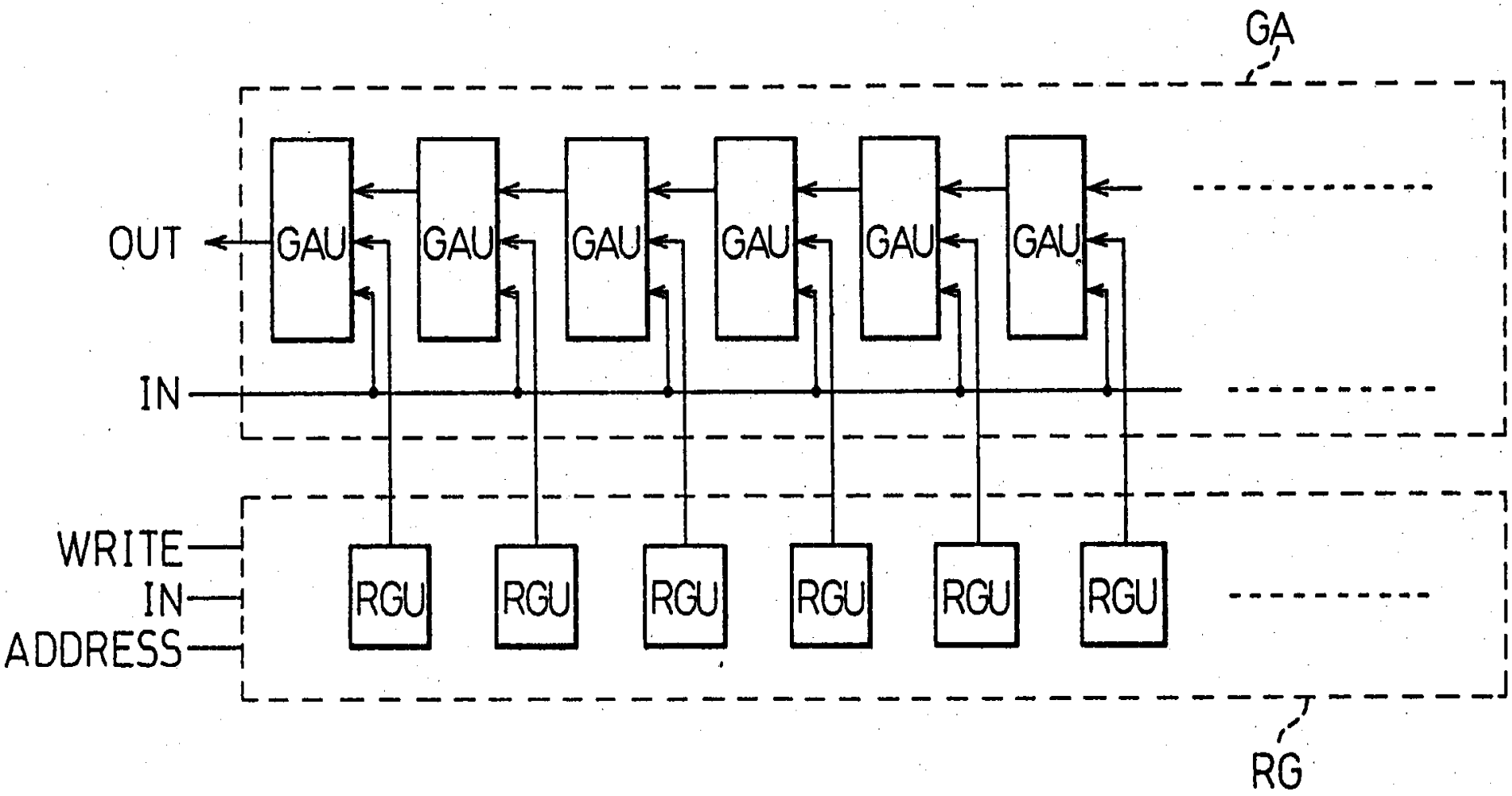

GA
OUT
GAU
GAU
GAU
GAU
GAU
GAU
IN
WRITE
IN
ADDRESS
RGU
RGU
RGU
RGU
RGU
RGU
RG

Fig.61

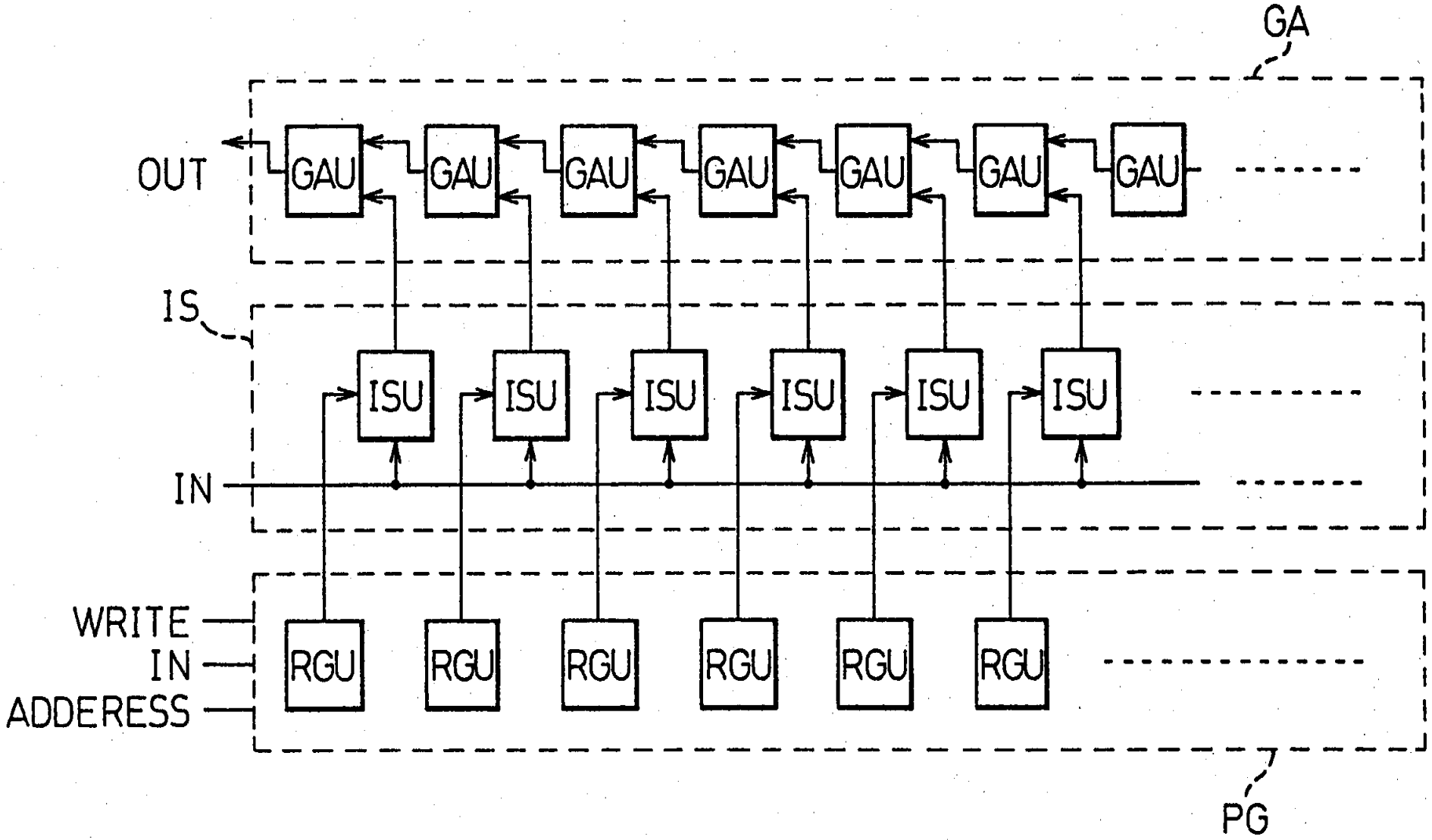

GA
OUT
GAU
GAU
GAU
GAU
GAU
GAU
GAU
IS
ISU
ISU
ISU
ISU
ISU
ISU
IN
WRITE IN
ADDERESS
RGU
RGU
RGU
RGU
RGU
RGU
PG

Fig.62

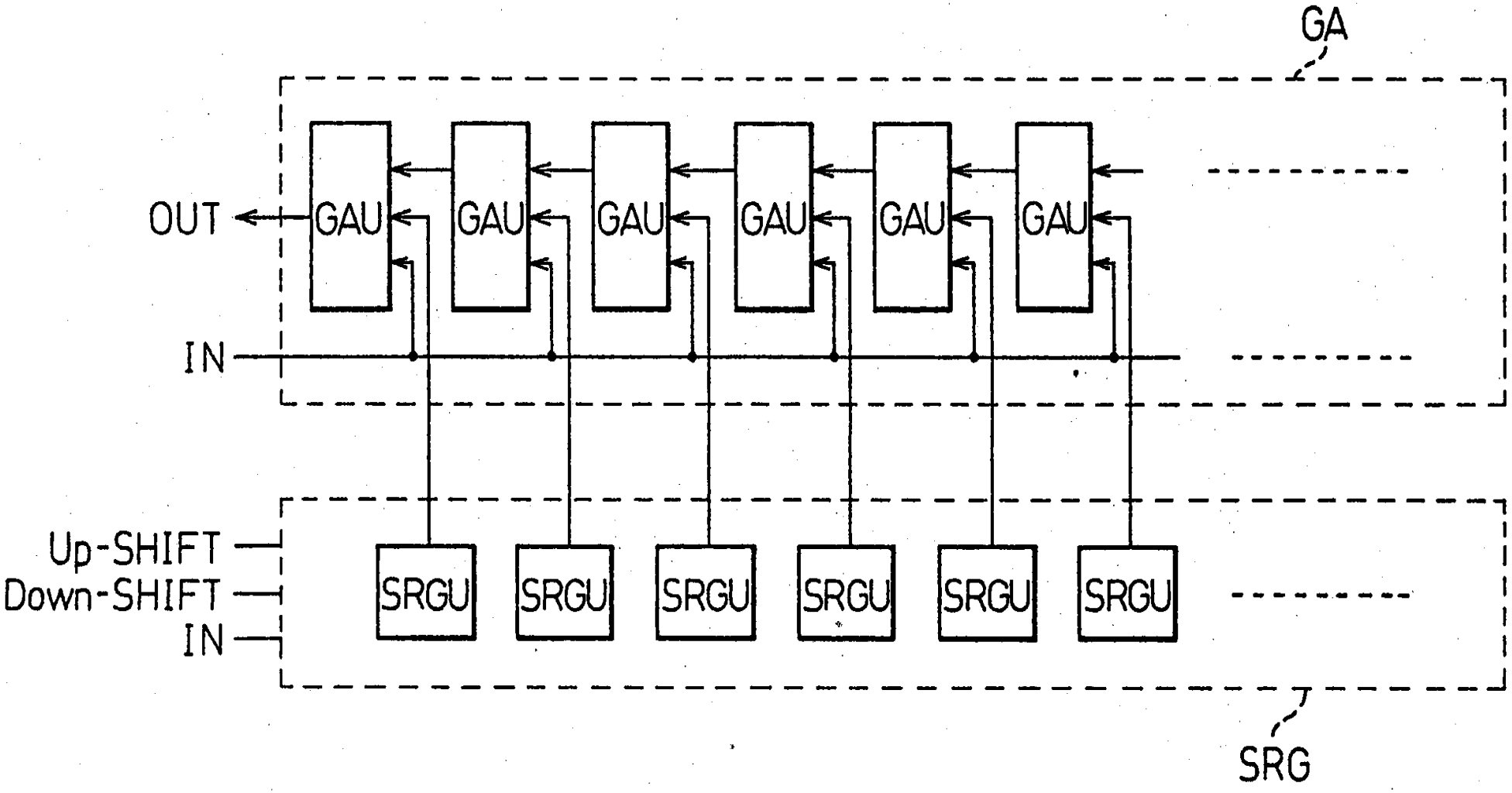

GA
OUT
GAU
GAU
GAU
GAU
GAU
GAU
IN
Up-SHIFT
Down-SHIFT
IN
SRGU
SRGU
SRGU
SRGU
SRGU
SRGU
SRG

Fig.63

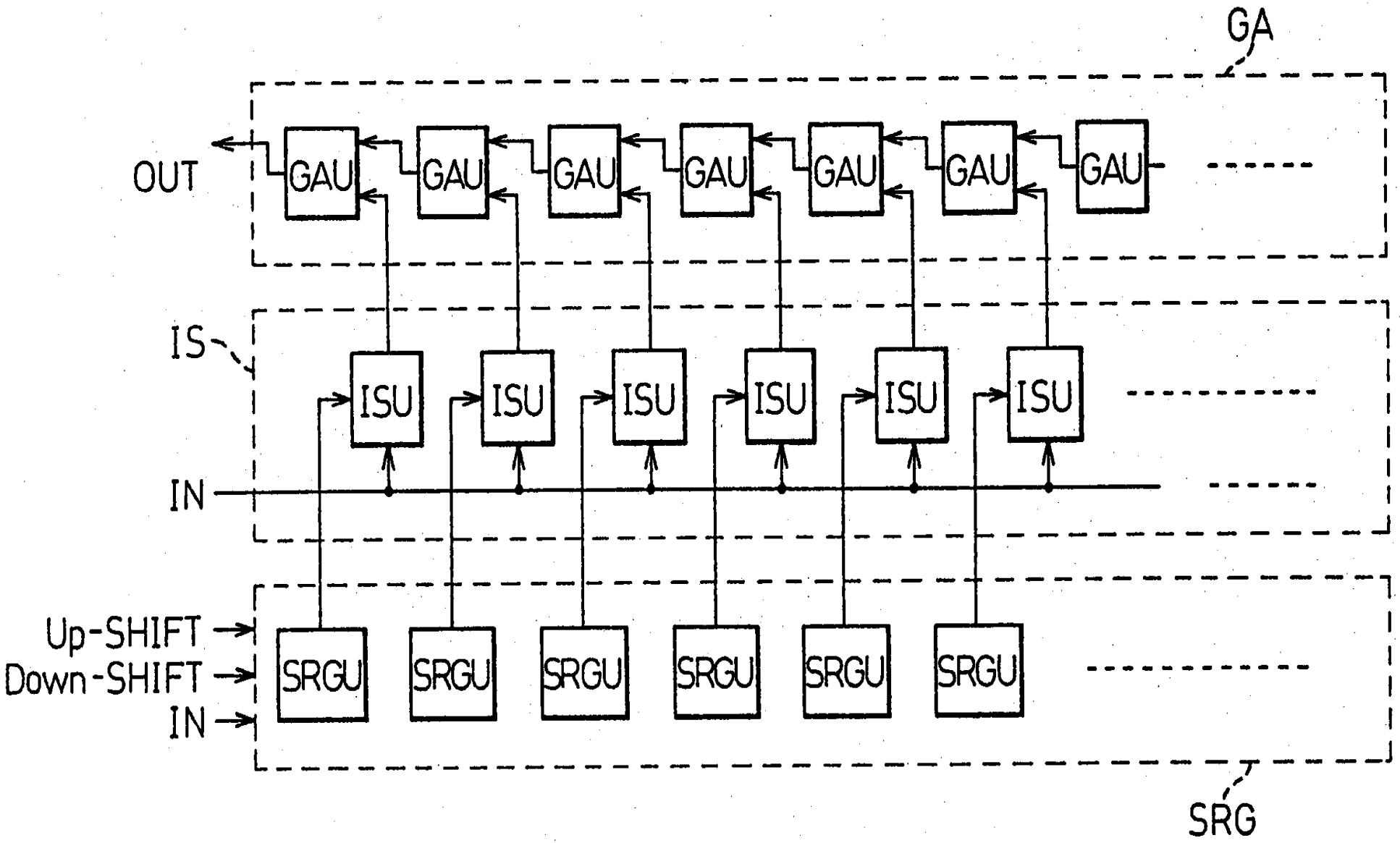

GA
OUT
GAU
GAU
GAU
GAU
GAU
GAU
GAU
IS
ISU
ISU
ISU
ISU
ISU
ISU
IN
Up-SHIFT
Down-SHIFT
IN
SRGU
SRGU
SRGU
SRGU
SRGU
SRGU
SRG

Fig.64

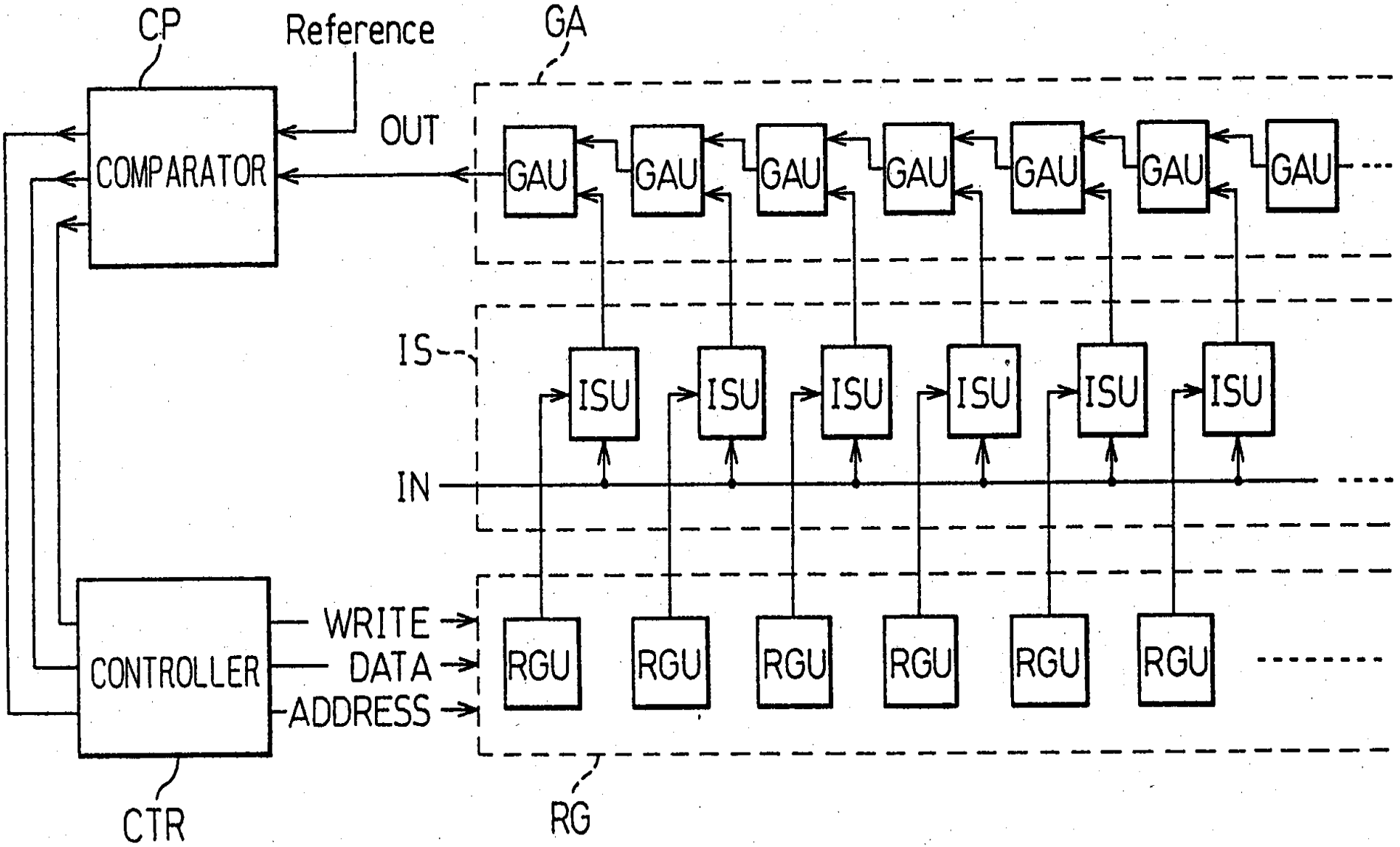

CP
Reference
GA
COMPARATOR
OUT
GAU
GAU
GAU
GAU
GAU
GAU
GAU
IS
ISU
ISU
ISU
ISU
ISU
ISU
IN
CONTROLLER
WRITE
DATA
ADDRESS
RGU
RGU
RGU
RGU
RGU
RGU
CTR
RG

Fig.65

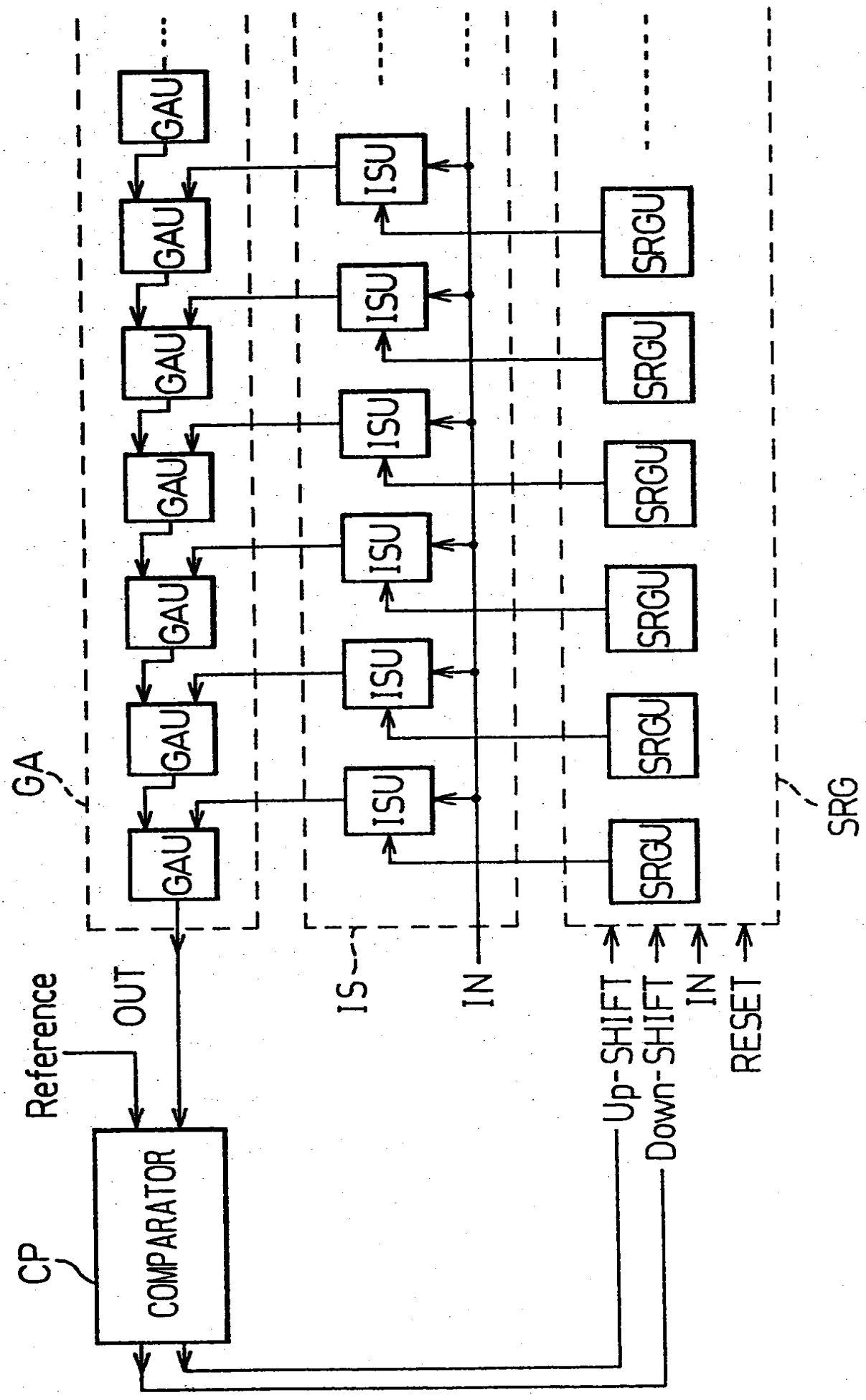

GA
GAU
ISU
SRGU
SRG
IS
IN
Up-SHIFT
Down-SHIFT
IN
RESET
OUT
Reference
CP
COMPARATOR

Fig.66A

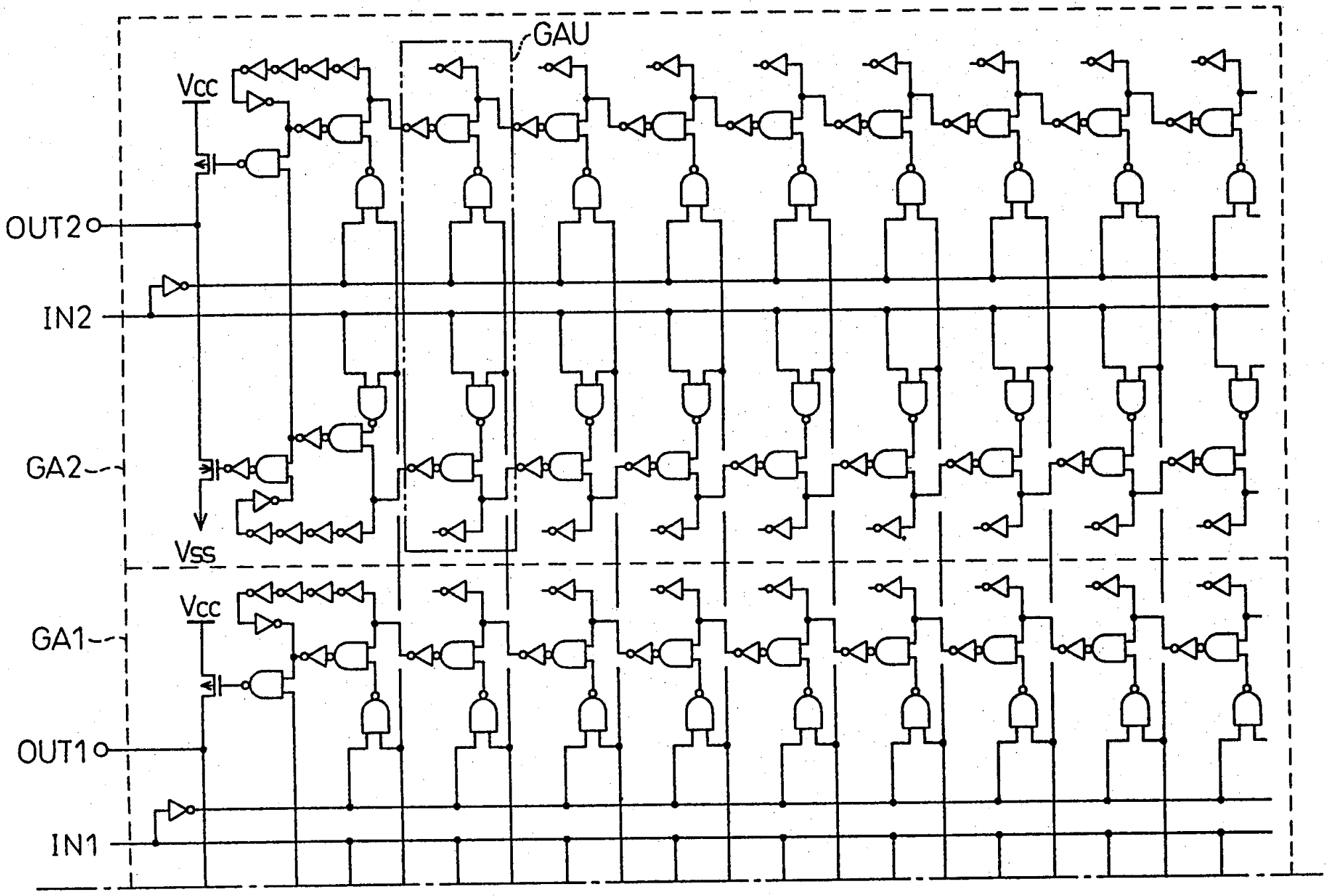


Fig.66B

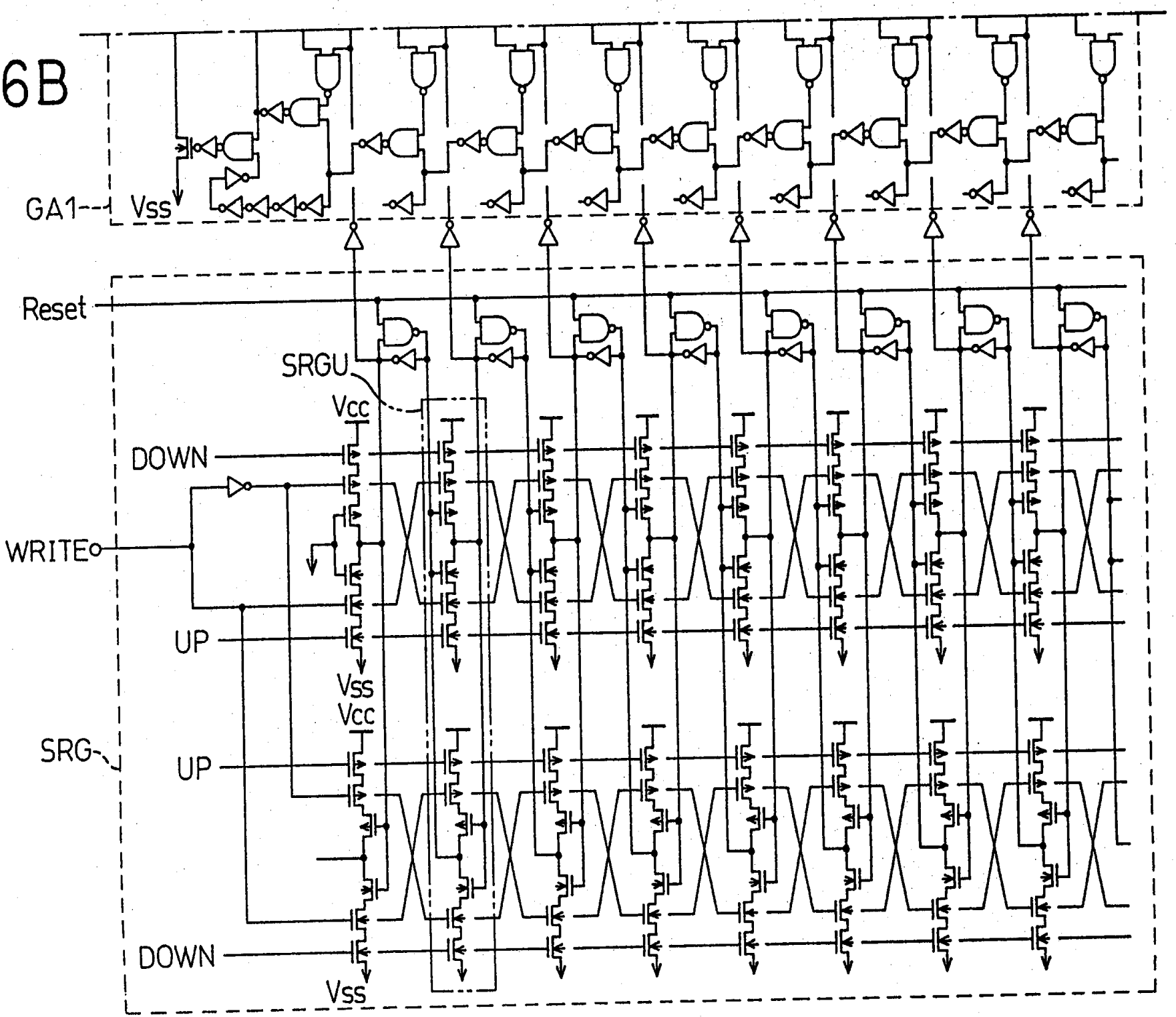
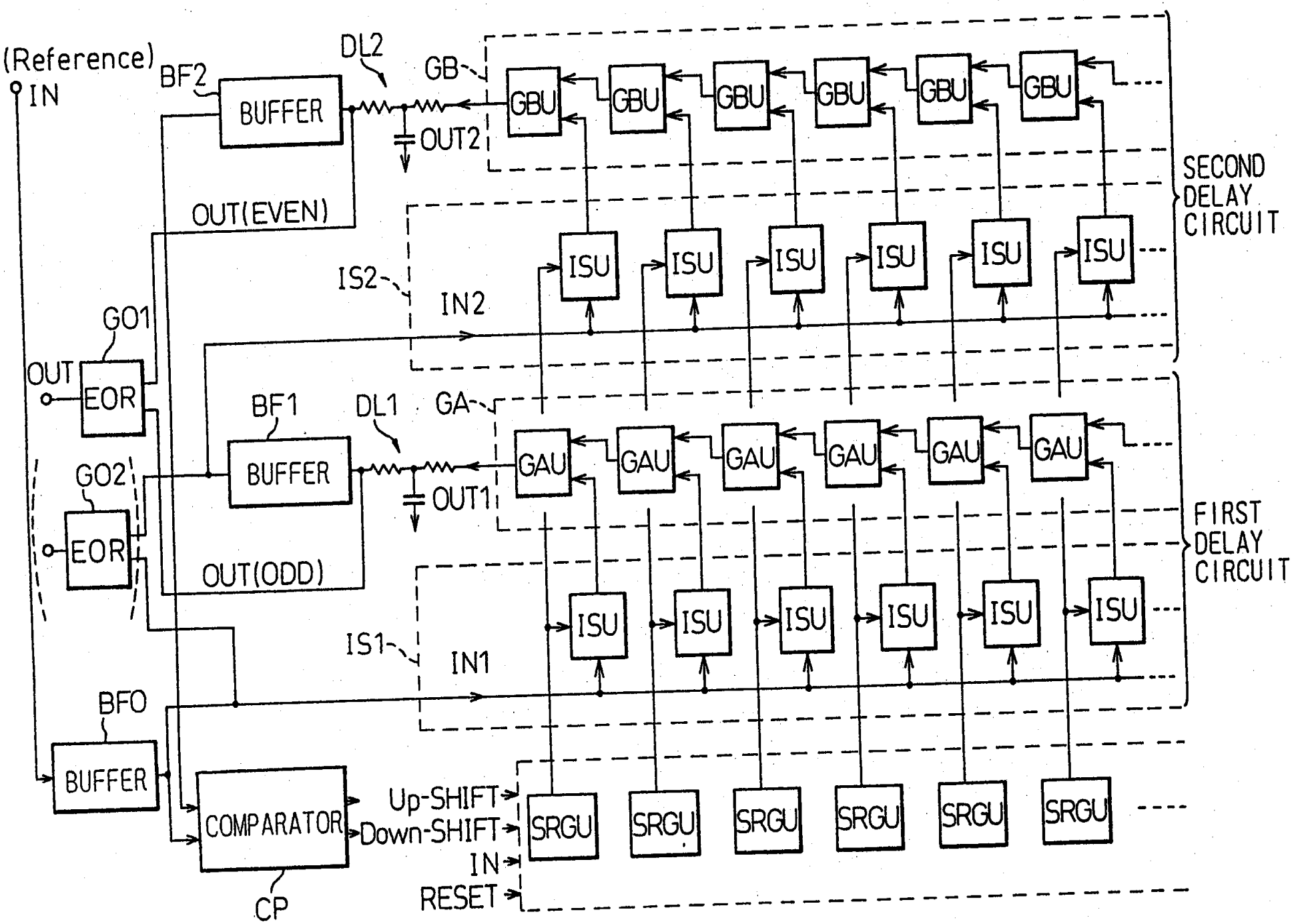


Fig.67


(Reference)
IN
BF2
BUFFER
DL2
GB
GBU
OUT2
OUT(EVEN)
SECOND DELAY CIRCUIT
ISU
IS2
IN2
GO1
OUT
EOR
BF1
DL1
GA
GAU
BUFFER
GO2
EOR
OUT1
OUT(ODD)
FIRST DELAY CIRCUIT
IS1
IN1
BFO
BUFFER
COMPARATOR
Up-SHIFT
Down-SHIFT
IN
RESET
SRGU
CP